MBE growth and characterization of InAs based core-shell nanowire arrays

Master thesis
in
Materials science

Author:
Doudou Wu
February. 2021

submitted to
Faculty of Georesources and Materials Engineering
of the
RWTH Aachen University

Supervisor:
1. Prof. Dr. Regina Dittmann
RWTH
2. Prof. Dr. Detlev Grützmacher
Dr. Mihail Ion Lepsa
PGI-10
Forschungszentrum Jülich GmbH

Abstract

Among III-V compound semiconductor nanowires, InAs nanowires have high electron mobility which make them suitable for low power field-effect transistors. The Fermi level pinning above its conduction band minimum results in easy fabrication of ohmic contacts. However, due to the large surface-to-volume ratio of nanowires, the surface states can have impact on the electrical property of InAs nanowires and therefore the influence of passivation is interesting to be investigated. The first part of this report focuses on the molecular beam epitaxy (MBE) growth of InAs nanowire arrays on prepatterned Si(111) substrates. Using a new in-situ Ga droplet assisted substrate preparation, a high reproducibility of the growth results with high nanowire yield is achieved. Afterwards, the in-situ passivation of InAs nanowire by Al_2O_3 shell using atomic layer deposition (ALD) is successfully realized. In addition, the MBE growth of InAs-$Al_{0.6}Ga_{0.4}Sb$ core-shell nanowire is studied and the growth rate of AlGaSb shell is estimated. The second part is related to the fabrication of InAs nanowire-array based device using HSQ as planarization layer. After the fabrication, each nanowire array as a whole is connected by top and bottom electrodes vertically. The third part contains the DC electrical characterization of the InAs nanowire-array based devices at room temperature. The comparison between the resistivity of unpassivated and Al_2O_3 passivated InAs nanowire arrays shows that the latter is lower demonstrating the benefit demonstrating the benefit of passivation.

Table of content

Introduction

Besides elemental semiconductor Si, III-V semiconductors which consist of elements from group III (Al, Ga, In) and from group V (N, P, As, Sb) are also of great importance for opto-electronic applications. In comparison with Si, III-V materials have some advantages: unlike Si which has indirect band gap, lots of III-V semiconductors exhibit direct band gap, for example GaAs, InP and InAs. III-V semiconductors with direct band gap enable direct recombination of electrons and holes which is suitable to build optoelectronic devices. For example, InP or GaAs based III-V semiconductor devices can be used for optical fiber communications, LEDs/LDs and solar cells [1]. In general III-V semiconductors have higher electron mobility than Si, especially the electron mobility of InAs is significantly high ($\leqslant$40000 $cm^2\ V^{-1}\ s^{-1}$ [2]). Therefore it is a good candidate for high electron mobility and low power consuming devices [3]. Additionally, not only binary but also ternary and quaternary compounds can be formed and as a result heterostructures with desired band gap engineering are easy to realize by changing the material compositions.

Nowadays with the development of integrated circuits, it is intensively investigated the continuous decrease of the transistor dimensions, in order to increase device density, improve logic performance and to reduce the power consumption [4]. However, traditional Si based field-effect transistors are reaching their physical limits. One of the potential improvements is to use novel device architecture, e.g. switching from planar channel to a nanowire channel with a cylindrical gate-all-around (GAA) architecture [5]. By this method, the gate control is improved and the short-channel effects can be minimized, therefore enabling a shorter gate length.

Nanowires have attracted great attention because of their unique one-dimensional nanostructures. Among III-V compound semiconductor nanowires, InAs nanowire is a good candidate to be used as high mobility channel for field-effect transistors due to its high electron mobility.

The integration of III-V compound semiconductors on a Si chip provides new possibilities for the design and fabrication of electronic devices. However, the lattice mismatch between Si and compound semiconductors restrains the integration. One solution is the growth of nanowires (typical diameter no more than 100 nm) using selective area epitaxy, which means the localized epitaxial growth of nanowires on Si substrate through a

patterned amorphous dielectric mask, such as SiO_2 [6][7][8]. The nanowires can grow from the designed holes with nanometer-scale size, which enables the integration of compound semiconductors and Si regardless of the lattice mismatch and thermal coefficients. In this thesis, the electrical properties of InAs nanowires are measured vertically on the Si substrate, on which the nanowires growth takes place.

To obtain the electrical properties of InAs nanowires, they are usually measured singly and laterally. This method is time consuming and needs high requirements for the lithography. It is interesting to measure the I-V characteristic of InAs nanowires not singly but measuring many nanowires simultaneously. This can be realized by measuring a nanowire array vertically. This method can also avoid big deviations between measurement results of individual nanowires and an average resistance value of single nanowire can be finally obtained.

In this thesis, first, the MBE growth of InAs nanowire arrays on prepatterned Si(111) substrate is studied, with the goal to obtain high yield of vertical nanowires and high reproducibility. Then the In-situ passivation of InAs nanowire with Al_2O_3 shell by ALD is studied. Afterwards, the InAs nanowire-array based devices are fabricated for two situations: InAs nanowires without any passivation and with Al_2O_3 passivation. Finally, the electrical characterization for the two situations is performed. The influence of Al_2O_3 passivation on InAs nanowire is discussed. Additionally, the growth of InAs/$Al_{0.6}Ga_{0.4}Sb$ core/shell nanowires by MBE is also presented.

1. Theoretical and technical background

1.1 Physical properties of InAs

InAs exhibits unique physical properties. It has narrow band gap (Eg=0.36eV at 300K), leading to low effective electron mass ($0.023m_0$) and high electron mobility ($\leq 4x10^4$ $cm^2V^{-1}s^{-1}$) [9], which makes it a good candidate for field-effect transistors with high speed and low power consumption. InAs nanowires can be used as channels for nanowire field-effect transistors [10].

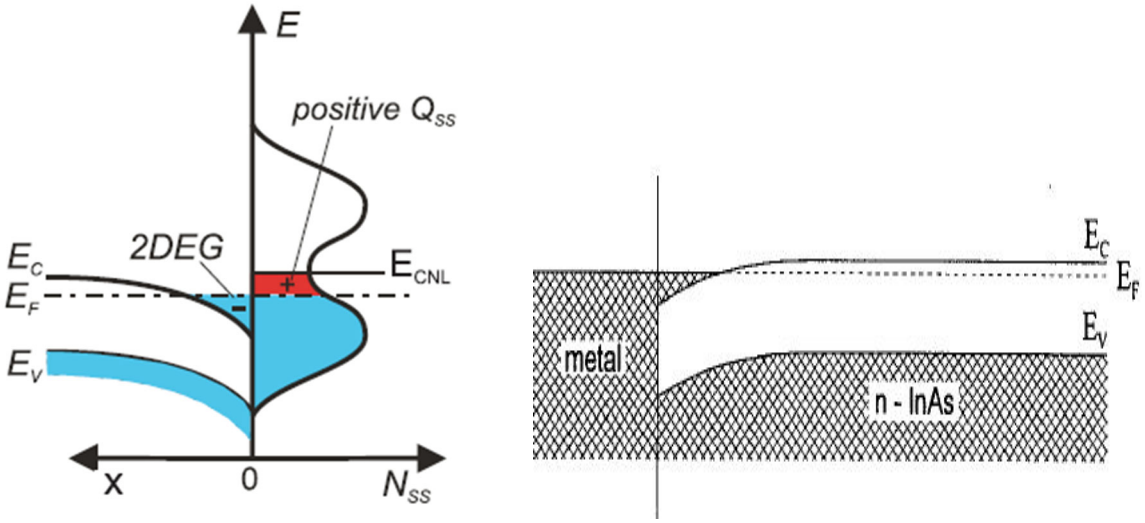
1.1.1 Crystal structure of InAs

Normally, the stable crystallographic structure of InAs bulk is zinc blende. Zinc blende structure can be seen as two face centered cubic lattices translated along the body diagonal by [1/4 1/4 1/4] a, where a is the lattice constant [11]. These two face centered cubic lattices are occupied by In and As respectively. The group III element In is at the position [0 0 0] while the group V element As is at the position [1/4 1/4 1/4]. The stacking sequence along [111] direction is ABCABC, according to the relative position of stacking layers. For nanowires, the stable crystal structure is a mixture of zinc blende and wurtzite [12][13]. The wurtzite structure has a hexagonal close packing structure with a basis of two types of atoms (In and As atoms). The stacking sequence is ABABAB along [0001] direction.

1.1.2 Surface properties of InAs

InAs has special surface properties. The surface atoms of semiconductor have less bonding partners, thus they do not have the same periodic structure as the bulk. Therefore, the energy structure of the surface is different from that of the bulk. When the surface density of states is extremely high, there is a surface Fermi level which is unchangeable and different from the bulk Fermi level, which is called Fermi level pinning. To achieve the thermodynamic equilibrium, the electrons move between surface and bulk. For InAs, the surface Fermi level pinning is above the conduction band minimum [14], thus the electrons transfer from the bulk to the surface. An electron accumulation layer is created at the surface so that a highly conductive 2-DEG (two dimensional electron gas) is formed at InAs surface. As a result, the intrinsic InAs is electrically conductive. The formation of the electron accumulation layer can be explained also by the Figure 1-1 (a), the electrons

are accumulated at the surface, because the charge neutrality level (E_{CNL}) of the surface is located above the bulk Fermi level, so that electrons from the donor like surface states are transferred to the bulk living behind the positive surface charge (Q_{ss}) to keep the charge neutrality [15]. The Fermi level pinning in the conduction band also leads to a metal-InAs interface which is ideally to realize ohmic contact with low resistance [16], which means that no potential barrier exists between metal and semiconductor. The energy band diagram is shown in Figure 1-1 (b).



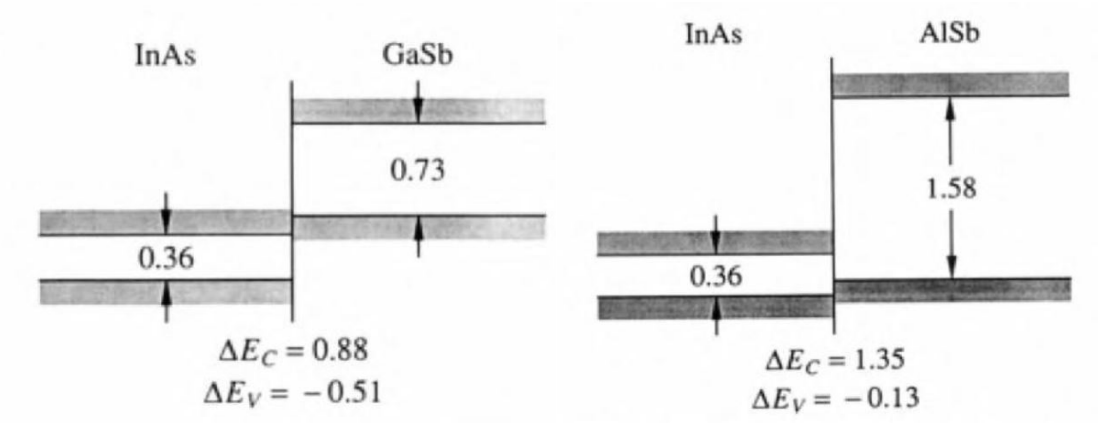
(a) (b)

Figure 1-1 (a) The band structure of InAs at the surface. The x axis refers to the distance to the surface and the N_{ss} axis refers to the surface state density per energy. Taken from [17]. (b) The band structure of metal-InAs contact.

As mentioned before, the surface states of InAs is an important factor to influence the transport properties. Compared with InAs bulk system, InAs nanowire has larger surface-to-volume ratio, so that the effect of the surface states on the transport properties of InAs nanowires can be significant [18]. They can result in a stronger ionized impurity scattering than bulk material. In addition, there is a strong surface roughness scattering. These factors can lead to a smaller electron mobility in the surface region [19]. Therefore, it is interesting to investigate the influence of surface passivation. In air atmosphere, a native oxide layer is created on InAs nanowire surface, which is however not a stable passivation layer. High k dielectrics such as Al_2O_3 can act as gate oxides or as a passivation of the nanowire surface. It is expected that with the in-situ Al_2O_3 passivation, the surface scattering can be reduced and the transport properties of InAs nanowire can be enhanced.

1.2 Heterostructure of InAs/AlGaSb core/shell nanowires

Growing radial nanowire heterostructures can create unique interface properties. There are three of types of III-V semiconductor heterojunctions, type I: straddling alignment, type II: staggered alignment and type III: broken-gap alignment. The experimentally determined band alignments for InAs/GaSb and InAs/AlSb are shown in Figure 1-2. The band alignment of InAs/$Al_xGa_{1-x}Sb$ can have a staggered or broken gap band alignment, which is dependent on Al content.



(a) (b)

Figure 1-2 (a) InAs/GaSb interface exhibits broken-gap alignment, (b) InAs/AlSb interface exhibits straddling alignment [20].

Because different materials have different lattice constants, the interface of heterostructure is normally lattice mismatched. Below critical thickness of shell, pseudomorphic growth is possible, while the structure is relaxed by the formation of dislocation beyond critical thickness, as shown in Figure 1-3. Therefore, it is necessary to know the critical thickness of researched structure. For core/shell nanowire, the critical thickness of the shell is dependent on the lattice mismatch degree of the material combination and the core radius. For InAs/AlGaSb, the lattice mismatch degree is very low (between 0.6%-1.2%). For planar structure, the critical thickness for GaSb is 20nm and for AlSb is 10nm according to the classical Matthews-Blakeslee theory [21]. But for InAs/AlSb as well as InAs/GaSb core-shell nanowires, the critical thickness with misfit-dislocation-free shell growth is at least twice as thick as for the planar structure, as discussed in [22]. For InAs/AlGaSb core-shell nanowires, dislocation-free shell thickness is expected to be larger than 20nm.

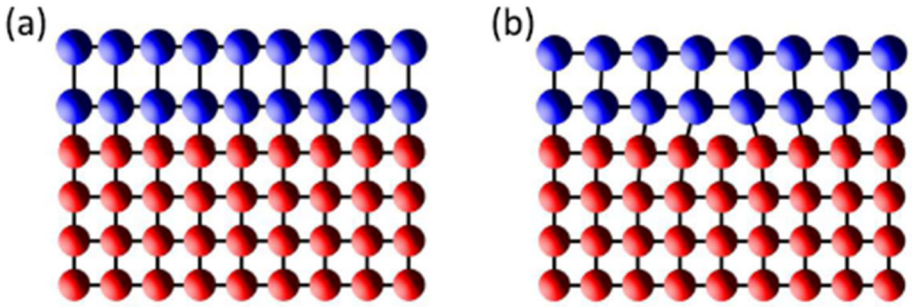


Figure 1-3 (a) Pseudomorphic growth and strained lattice structure (b) Dislocation formation and relaxed lattice structure. Taken from[23].

1.3 Growth and characterization techniques

1.3.1 Molecular Beam Epitaxy

Molecular Beam Epitaxy (MBE) is used in this thesis to grow InAs nanowires and InAs/AlGaSb core/shell nanowires. MBE is one of the fundamental tools to grow epitaxial semiconducting materials. The schematic is shown in Figure 1-4. The elemental materials are heated separately in effusion cells to a temperature where the elements can evaporate or sublimate. MBE requires ultra-high vacuum (typically 10^{-10} mbar), this extremely low chamber pressure ensures the purity of deposited materials and also ensures a long mean free path of evaporated atoms. The evaporated atoms therefore will not react with each other in chamber but only on the substrate. The fluxes of materials, which determine the deposition rate to a great extent, are controlled by cell temperatures. The group V materials As and Sb are stored in the reservoirs of valved cracker sources. The fluxes can be adjusted by valve position and reservoir temperature. Arsenic is supplied mainly as As_4 or As_2 depending on the cracker temperature. When the cracker temperature is 600°C, arsenic evaporates from cell as As_4, while arsenic evaporates from cell as As_2, when the cracker temperature is 900°C. In this report, the cracker temperature is set at 600°C.

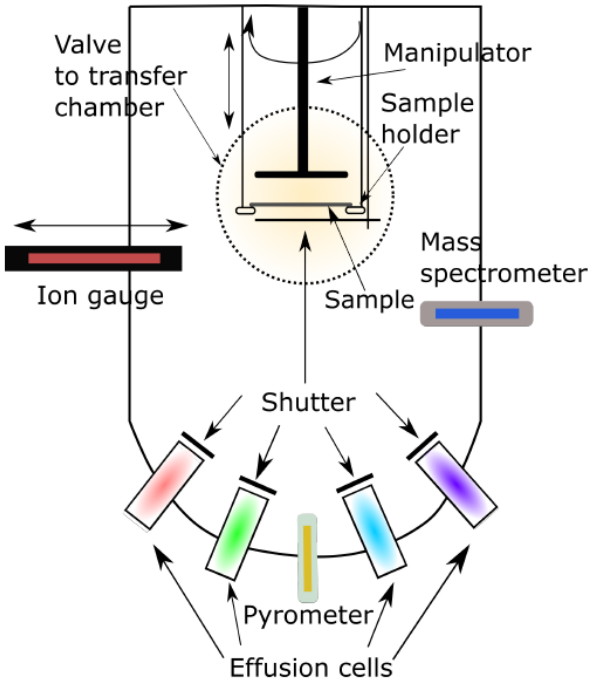


Figure 1-4 Schematic of the principal parts of a typical molecular beam epitaxy reactor (MBE). Taken from [24].

The fluxes of elements are proportional to the beam equivalent pressures (BEPs), which are measured with ionization gauge All the cell temperatures can be regulated by a software program.

1.3.2 Atomic layer deposition

Atomic layer deposition (ALD) is a vapor-phase deposition technique which can be used to grow high-quality thin film, e. g. high κ films such as Al_2O_3 and HfO_2. The ALD technology is based on a sequential, self-limiting surface chemistry. During the growth, the precursor and co-reactant are offered into reactor alternatively. As shown in Figure 1-5, precursor A is added into the reactor first and one layer of precursor A is deposited on the substrate surface. Then the reactor is purged in order to get rid of all residual precursor from the reactor. Afterwards, the co-reactant B is inserted to react with the layer of precursor A. The reaction happens at the sample surface in a self- limited way. Finally, the chamber is purged again. These four steps constitute an ALD cycle. After one cycle, one atomic layer of required material is generated. The thickness of material depends on the number of cycles. The thickness can be precisely controlled at the sub-nanometer

level by varying the cycle numbers. The ALD process happens at relatively low temperature with high uniformity and conformality [25]. These benefits make ALD an attractive method for semiconductor applications.

In this thesis, to deposit Al_2O_3 layer by ALD, precursor A represents trimethylaluminum (TMA, $Al(CH_3)_3$) and co-reactant B represents H_2O.

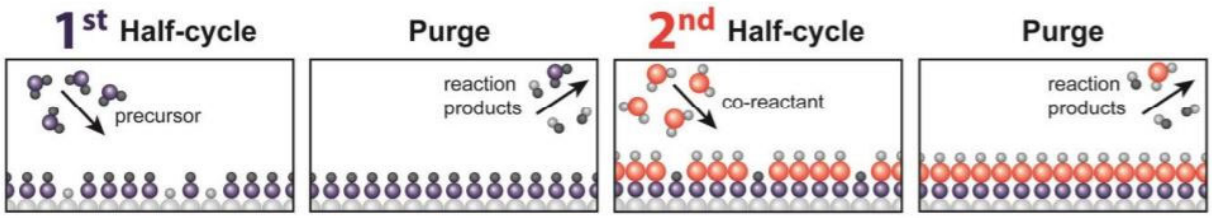


Figure 1-5. Schematic of an ALD cycles. The first half-cycle describes the deposition of precursor and the second half-cycle describes the deposition of co-reactant, with a purge process in between. The exposure time need to be sufficient to get saturated growth, and the purging time also need to be sufficient to avoid the reaction of the precursor and co-reactant directly in the gas phase. Adapted from [25].

1.3.3 Scanning electron microscopy

Scanning electron microscopy (SEM) is the most used characterization technique in this study to inspect the morphology of grown nanowires and fabricated devices. In high vacuum conditions, a focused electron beam scans the specimen surface. The electrons interact with the atoms of the specimen and produce various kinds of signals including secondary electrons (SE), back-scattered electrons (BSE), characteristic X-rays etc. Topography information can be obtained by the SE mode. In this mode, low-energy electron beam interacts with sample inelastically and secondary electrons are excited from surface or near surface regions. The information of secondary electrons are detected by secondary electron detector. In the SE mode, topographical image with resolution less than 0.5nm is possible to obtain. Additionally, for conventional SEM imaging, specimens need to be electrically conductive, because nonconductive specimens will collect charges during electron beam scanning and it will be difficult to obtain accurate surface topography images.

1.3.4 Ellipsometry

Spectroscopic ellipsometry is used to determine the optical constants and the thickness of thin films. In this study, the thickness of thermal SiO_2, PMMA, HSQ, AZ5214E and Al_2O_3 deposited by ALD are all obtained using the ellipsometer.

During measurements, the incident beam interacts with material structure (e. g. reflection, absorption, scattering and transmission can happen), the polarization of light will be changed afterwards due to different optical properties of material and different film thickness. The change of polarization is parameterized by the amplitude ratio Ψ and the phase change difference Δ. Afterwards, a data analysis must be performed using the correct layer optical model and layer sequence. As a result, the thickness of layers can be calculated.

1.3.5. Atomic force microscope

Atomic force microscope (AFM) technology is based on the atomic force between tip and sample to explore the topographic information of the sample surface in the nanoscale range. A sharp tip is mounted at the free end of the cantilever. During scanning, the position detector records the deflection of the cantilever through a laser beam reflection change. There are three traditional modes of AFM: contact mode, non-contact mode and tapping mode. In contact mode, the tip of AFM is touching the surface during measuring and the deflection changing of the cantilever is the feedback value. In non-contact mode, the tip and the sample are not in contact each other, the cantilever always oscillates at resonance. In tapping mode, the tip and the sample have an intermittent and short contact during scanning, the cantilever oscillates at a fixed driving frequency which is at or very close to the free resonance frequency. The change of amplitude is dependent on the tip-sample distance monotonously. The amplitude change is set as feedback signal in this method. The disadvantage is that the force between tip and sample is hard to control, which could lead to damage of the sample. Another mode---peak force tapping mode, which was launched by Brucker in 2010 is superior. In this mode, the tip-sample distance is modulated in a sinusoidal motion, which means the closer the probe to the sample surface, the slower is the motion of the probe relative to the sample surface. This feature ensures the accurate control of the tip-force interaction. The tip-sample interaction is controlled by maintaining the peak force (pN-level) between tip and sample constant The peak force is measured by the deflection of the cantilever. This method provides high-resolution imaging and protects the sample and as well as the tip from damage. In this

study, the depth of the holes on prepatterned SiO_2/Si substrate is determined by AFM using peak force tapping mode.

1.4 Metal-semiconductor contacts

In this thesis, in order to measure the I-V characteristic of InAs nanowire arrays, metal-semiconductor contacts are fabricated. Therefore, it is of importance to understand metal-semiconductor contacts and their influences on I-V characteristics of nanowires. Basically, there are two kinds of metal-semiconductor contacts: Schottky contact and ohmic contact.

1.4.1 Schottky contact

When metal and semiconductor get into contact, the energy band diagram of the metal and the semiconductor are aligned using the same vacuum level, and the Fermi levels of the two materials are misaligned due to different work functions. Then, the charge carriers will move from one material to the other until they reach the thermal equilibrium. For example, for an n-type semiconductor, if its work function $\boldsymbol{\Phi_m}$ is smaller than that of the work function of the metal $\boldsymbol{\Phi_s}$, as shown in Figure 1-6, the electrons will flow from semiconductor to metal until reaching the thermal equilibrium, which will result in a depletion layer at the interface of the semiconductor side. Accordingly, the energy band structure is bent upwards and a potential energy barrier is built at the interface. This kind of contact is named Schottky contact. The barrier height $\boldsymbol{\Phi_B}$ is the difference between metal work function $\boldsymbol{\Phi_m}$ and the electron affinity χ of the semiconductor. The electron affinity χ and the metal work function $\boldsymbol{\Phi_m}$ are invariant values depending only on the materials which will not change during contacting.

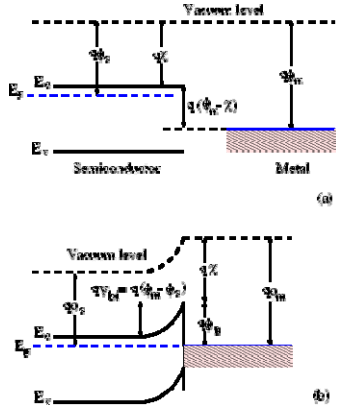


Figure 1-6 (a) Energy band diagram of a metal adjacent to n-type semiconductor under thermal non-equilibrium condition. (b) metal-semiconductor contact in thermal equilibrium. Taken from [26]

Such a Schottky contact has rectifying property: under forward bias (V>0, a positive voltage V is applied on the metal and the semiconductor is connected to the ground.), the Fermi energy of the metal becomes lower than the Fermi energy in the semiconductor, the potential barrier from the semiconductor side is lower, which means that it is easier for electrons in the semiconductor to flow into the metal. As a result a large current is achieved. While under reverse bias (V<0, a negative voltage V is applied on the metal and the semiconductor is connected to the ground.), potential barrier becomes larger, the diffusion of electrons from semiconductor to the metal will be blocked. Only a small amount of thermally excited electrons in the metal is able to overcome the potential barrier and the corresponding current is very small. At very high reverse biases, the depletion region breaks down and the current becomes extremely large. The changed energy band structure is shown in Figure 1-7 (a) and (b). In general, the relationship between current flowing through the Schottky contact and the applied voltage can be described as:

$$I=I_0\,(e^{qV/kT}-1) \qquad (1.1)$$

Where I_0 is the saturation current, V is the applied voltage, q is the electronic charge, T the absolute temperature and k the Boltzmann constant. The typical I-V characteristic of a Schottky contact is shown in Figure 1-7 (c).

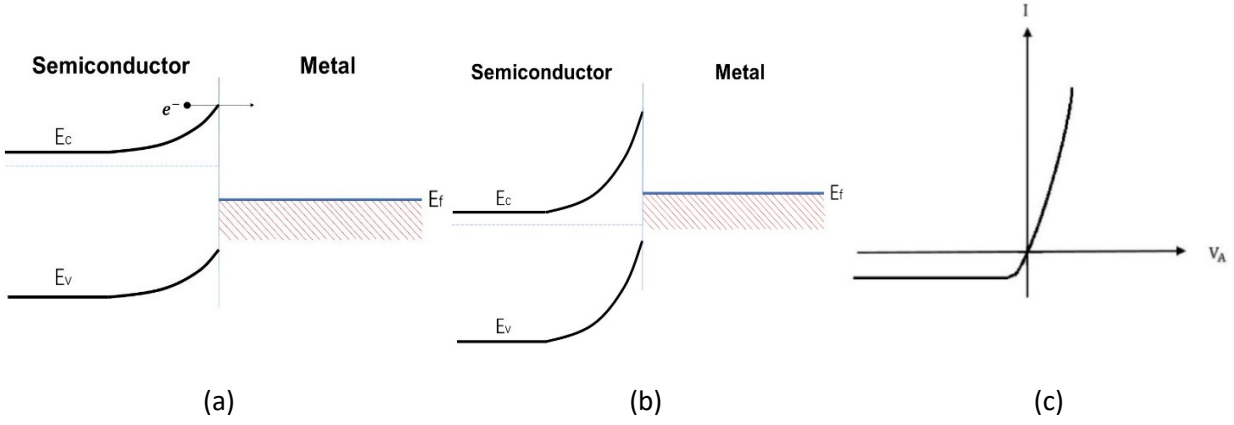


Figure 1-7 (a) The band structure at Schottky contact interface under forward bias. (b) The band structure at Schottky contact interface under reverse bias. (c) I-V characteristics of a Schottky contact.

1.4.2. Ohmic contact

In order to gain the electrical properties of InAs nanowires, the metal-semiconductor contact resistance should be minimized, and Ohmic contacts should be realized. An ideal Ohmic junction has low resistance and non-rectifying property which means no potential

barrier exists between the metal-semiconductor interface. The transformation of Schottky contact into ohmic contact can be realized by lowering the potential barrier or making the barrier very narrow by doping it heavily.

In this thesis, the Ti/Au-InAs top contact is ohmic because the Fermi level pinning of InAs results in a negative potential barrier and there is an electron accumulation layer at the InAs surface. Therefore, the electrons in InAs and metal can flow into each other without barrier, as clarified in section 1.2.2. The Ti/Au-silicon bottom contact is also ohmic because the silicon substrate is heavily n-doped, thus, the potential barrier is very thin and electrons can tunnel through the thin barrier.

2. Selective growth of InAs-based nanowire arrays by MBE

2.1 Selective growth of InAs nanowire – old method

2.1.1 Substrate preparation

An appropriate substrate preparation is essential to obtain high yield of vertical InAs nanowires-. First, the substrate preparation process from [27] and [28] was followed and is modified afterwards. The detailed process is illustrated in Figure 2-1 and is described as following:

a) The 4 inch n-doped Si (111) wafers are wet chemically cleaned in Piranha solution (96% H_2SO_4: 37% H_2O_2 = 3:1 in volume) for 10min to get rid of organic contaminants and rinsed in DI water also for 10 min. Then, the wafers are cleaned with 1%HF solution for 10mins to remove native oxide. After each step, they are dipped into DI water for 10min. The wafers are transferred afterwards into the oxidation furnace for the growth of 20nm thermal oxide. The thickness of silicon dioxide is measured by ellipsometry in general obtaining the desired value, 20±1 nm. To protect the surface during dicing, the wafers are spin-coated with resist AZ5214E at 6000rpm (acc. 4000rpm) for 30s and then soft bake at 90°C for 5min. Afterwards the wafers are diced into 2.5x2.5cm^2 samples. The AZ5214E resist is then cleaned with ultrasonic bath with acetone for 10min and isopropanol for 5min. The schematic of the substrate after this step is shown in Figure 2-1 (a).
b) Afterwards, the samples are spin-coated with resist PMMA 950K 679.04 at 6000rpm for 60s and baked at 180°C for 10min, as shown in Figure 2-1 (b). In order to enhance the adhesion between PMMA and Si/SiO_2 substrate, a priming process using hexamethyldisilizane (HMDS) at 130°C is performed prior to PMMA spin coating. The thickness of PMMA is 220nm±10nm after baking: This can vary with PMMA storage time, long storage time leads to higher PMMA thickness due to less solvent inside.
c) Then, the samples are sent to do the electron beam lithography (see Figure 2-1 (c)) using the writing pattern and expose doses from [28], as shown in Figure 2-2 and Table 2-1. Next, the samples are dipped into AR-60055 for development for 70s and transferred into isopropanol for 3min to stop the development.

d) To remove possible residual resist in the pattern holes, 15s oxygen plasma cleaning (300W, 200sccm) at Giga batch is used. Afterwards the samples are transferred to the reactive ion etching (RIE) chamber. The gas CHF_3 (50sccm) is used in RIE process at working temperature 20°C. Because the thickness of SiO_2 is ~ 20 nm, the etching depth need to be larger than 15nm but smaller than 20nm in order not to damage the Si surface (see Figure 2-1(d)). The RIE time determination will be discussed in session 2.1.3.

e) The left SiO_2 inside the holes is finally removed by using an 1% HF solution (see Figure 2-1(e)).

f) The PMMA resist is removed by acetone (6min) and isopropanol (2min) using ultrasonic bath. 10min oxygen plasma cleaning (300W, 200sccm) at Giga batch is used afterwards to ensure a resist-free surface. The samples are cleaned again 10min in Piranha solution) and rinsed in DI water for 10min. To remove the oxide resulted during Piranha cleaning, the samples are dipped 1 min into 1% HF solution exposing the bare silicon surface inside the holes (see Figure 2-1(f)).

g) The samples have to be loaded into the load lock chamber of the MBE system within 30min to avoid re-oxidation of Si surface. In the load-lock chamber the samples are baked at 200°C for 45min. Then, they are transferred into the preparation chamber and baked at 700°C for 1h. Now, they are ready for nanowire growth in the MBE chamber.

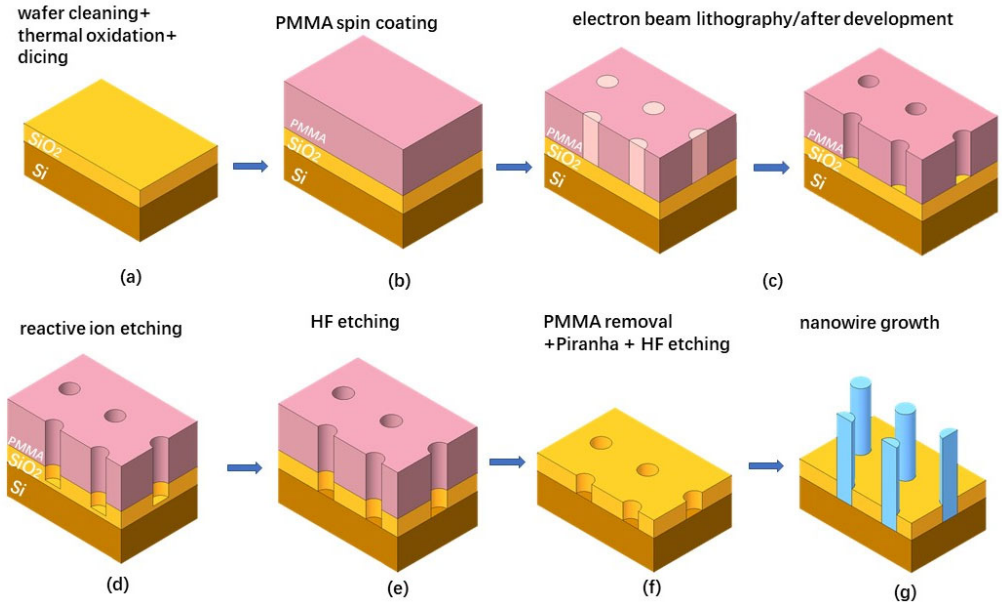


Figure 2-1. Schematic of the substrate preparation process.

Table 2-1 Electron beam dose used for different hole diameters.

Hole diameter (nm)	Exposure dose ($\mu C/cm^2$)
20	1344
40	544
60	410
80	350

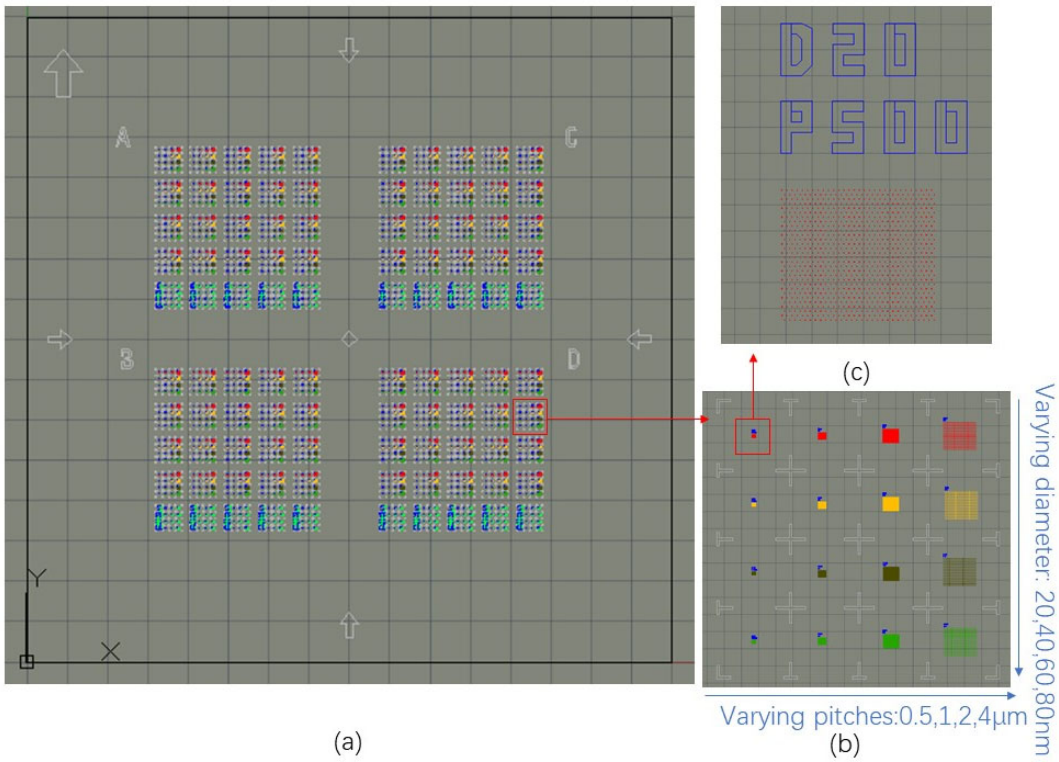


Figure 2-2. AutoCAD electron beam lithography mask from[28] (a) the whole pattern on the 2.5x2.5cm^2 sample. There are four identical parts, A, B, C and D, and each part consists of 4x5 square areas with hole arrays. The last row of each part contains special patterns which is not used in this thesis; the other four rows have identical square areas. (b) close-up of one of the square areas, which contains 4x4 nanowire arrays with pitches (distance between holes) 0.5 μm,1 μm,2 μm,4μm and hole diameter 20nm,40nm,60nm,80nm. (c) close-up of one of the nanowire arrays: D20P500 (D: diameter, P: pitch), the red points are the holes. There are totally 900 holes (30*30) in one nanowire array.

2.1.2 Growth mechanism of InAs nanowires

Two growth methods without any foreign catalyst, e. g. Au, have been investigated before: (a) vapor-liquid-solid (VLS) mechanism, in which the group III element acting as self-catalyst [29] and (b) vapor-solid (VS) growth mechanism which does not require any catalyst but the nanowires are self-seeded [30]. The second method is adopted in this thesis. The mechanism is shown schematically in Figure 2-3. The In atoms and As_4 molecules are evaporated from effusion/cracker cells and impinge on the substrate surface. The prepatterned holes, in which bare Si surface is exposed, are suitable to serve as nucleation sites since the sticking coefficient of In adatoms on Si(111) is much higher than on SiO_2 [31]. Then, the growth is continued by absorbing adatoms which diffuse along the surface or through direct incorporation of the impinging species. This results in the radial and axial growth of the nuclei and they finally turn into InAs nanowires. Besides the material fluxes, the substrate temperature is also important to determine the nanowire growth rate. At high temperatures, decreased nanowire length is observed due to increased thermally activated In adatom desorption and increased thermal decomposition of InAs [6][31][32]. On the other hand, at low temperature, the nanowire length is also inhibited due to the reduced diffusion length of In adatoms and therefore higher sticking coefficient, so that the incorporation rate contributing to nanowire growth is also lower. For InAs nanowire, as discussed in [6], the optimal growth temperature window is 480-510°C. In this thesis, 480°C and 460°C are used, with which good results can obtain. The substrate temperature is measured by a thermocouple and accurately controlled by dedicated controllers. The controller parameters and temperature can be set remotely using a computer software.

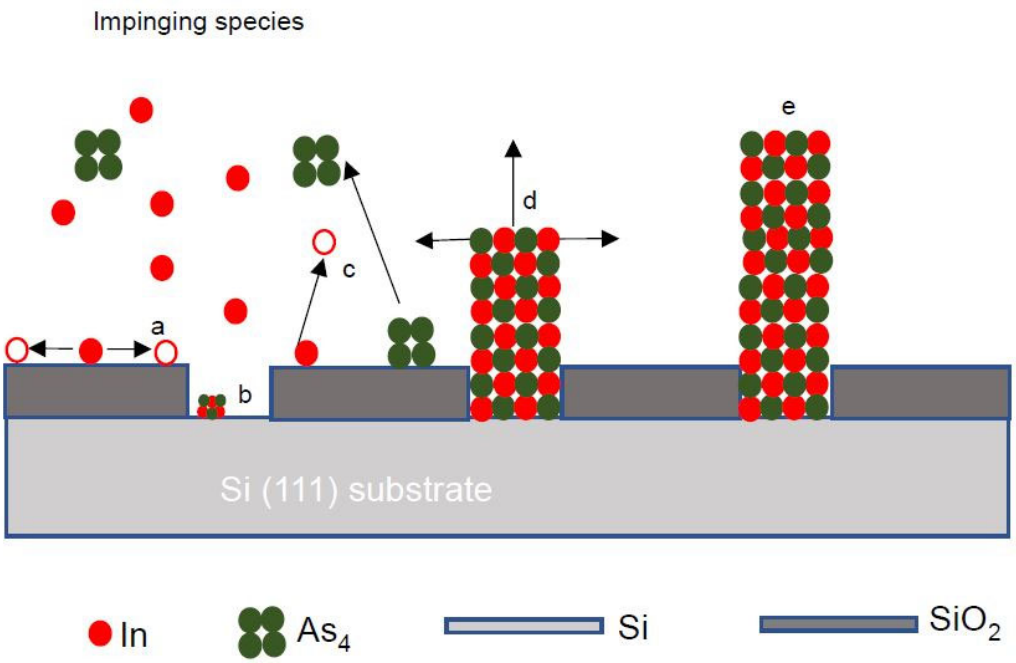


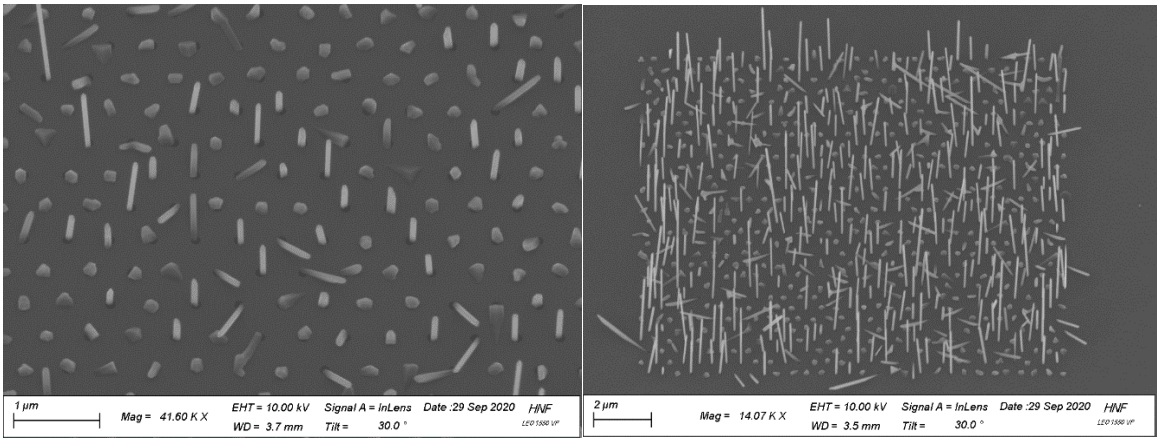
Figure 2-3. Schematic of InAs nanowire growth. (a) Surface diffusion of In atoms, for confining into holes (b) Formation of critical nuclei (c) Desorption of In and As from the oxide surface (d) Nanowire starts to grow in the radial and axial directions (e) Nanowire growth. Taken from [28]

The MBE growth recipe is as followed: First, the substrate temperature is set at 480°C with As beam equivalent pressure (BEP) of 4×10^{-5} mbar for 10min. Then, the In shutter is opened, the flux corresponding to a growth rate of 0.08 μm/h (determined by the growth rate of a planar InAs layer). the As BEP remains at 4×10^{-5} mbar and the nanowire growth starts. After 10 min growth, the substrate temperature is reduced to 460°C in 5 min. Simultaneously the In rate is reduced to 0.03 μm/h and As BEP is reduced to 2.5×10^{-5} mbar. This growth conditions are maintained until the end of the growth and the corresponding time is defined as the growth time and determines the nanowire length. In this recipe, the higher In rate and As flux at the beginning aim to facilitate nucleation and the lower In rate and As flux afterwards aim to restrain the lateral growth of nanowires [27].

2.1.3 Problems regarding to growth results

To investigate the influence of different RIE etching time on nanowire growth, two substrates are fabricated with RIE time 110s and 150s respectively. 150s is the previous parameter used in our institute to etch 15nm SiO_2 inside the holes. 110s is newly estimated, which is the time needed to etch 15nm SiO_2 inside the holes, under the

estimation that the etching rate inside holes is 60% of the etching rate on a planar SiO_2 layer (planar etching rate: 0.23±0.025nm/s). The growth results are shown in Figure 2-3.



(a) (b)

Figure 2-4. (a) Nanowire growth with RIE time 110s and growth time 3h (region D80P500) (b) Nanowire growth with RIE time 150s and growth time 2h30min (region D60P500).

By comparing the SEM images of the two samples, it can be seen that the RIE time 110s might be not enough. As seen in Figure 2-3 (a), the yield of vertical nanowires is less than 30% and there is a large amount of crystallites. The formation of crystallites instead of nanowires might be due to residual silicon dioxide in the bottom of the holes, so that the axially epitaxial growth can hardly accomplish resulting in crystallite growth, or can only accomplish very late, which leads to the formation of short nanowires (most of them are not longer than 500nm). In comparison, on the sample with RIE time 150s, long nanowires have grown even though the growth time is with 30min shorter than for the other sample, which at least means that the RIE time is more suitable, the nucleation occurs easier and InAs nanowires start to grow earlier. However, the yield of vertical nanowires is not more than 50%, and there are many tilted nanowires and crystallites, which is not suitable for nanowire-array based device fabrication. Another problem for both samples is that there are some empty holes after the growth for hole diameters of 20, 40, 60 nm, which afterwards is proved that it is due to much lower In flux than desired value, rather than insufficient electron beam doses. Insufficient In flux results in less nucleation probability and therefore, there are many empty holes.

Two approaches are used to improve the yield of vertical nanowires. The first approach is to modify the RIE time. Insufficient RIE time leads to problems with nucleation, but too long RIE time can damage Si surface which might also lead to crystallite growth.

Therefore, it is important to find out a suitable RIE time. To clarify the hole depth after RIE, 3 samples were processed with RIE time 130s, 140s, 150s respectively. After RIE process, the hole morphology is measured with AFM. The hole profiles are shown in Figure 2-5. The average hole depth is shown in table 2-2. 150s RIE etching time gives a hole depth slightly higher than 20nm, which means there is almost no SiO_2 left inside the holes, the silicon surface is probably damaged, which could be the reason why the sample with RIE time 150s presented in section 2.1.3 has low vertical nanowire yield. The RIE etching time of 130s was considered in the subsequent experiments. An average hole depth of 17.25nm in average and is supposed to provide an undamaged silicon surface.

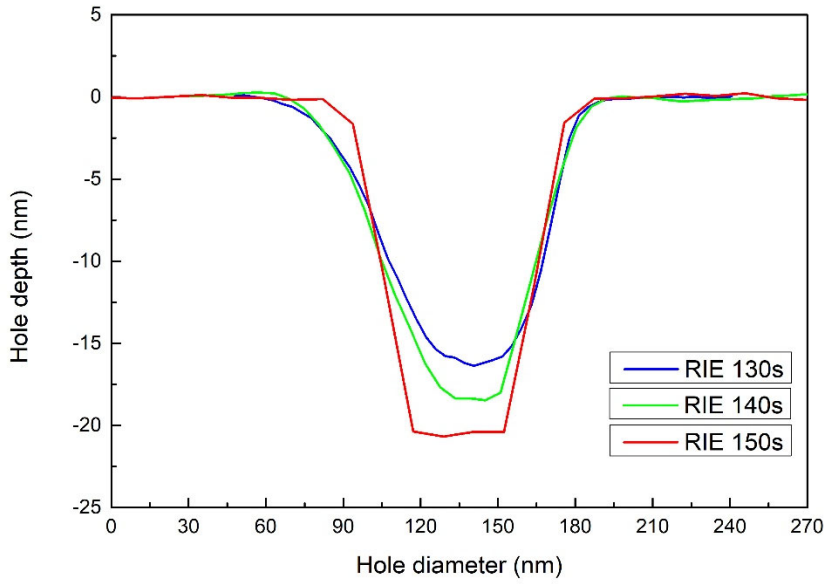


Figure 2-5. The hole morphology after different RIE times under AFM measurement.

Table 2-2

RIE time/s	Hole depth in average/nm
130	17.25±0.33
140	18.47±0.39
150	20.30±0.21

The second approach is related to the re-calibration of the In flux (growth rate). Much lower In flux than desired in the growth experiments presented at the beginning of this section is due to an incorrect correspondence between the In effusion cell temperature and In deposition rate. A correct calibration of the In growth rate is the precondition to get

reliable growth results. RHEED (Reflection high-energy electron diffraction) is used to make the calibration.

The experiment for In growth rate calibration was carried out on a GaAs substrate. The substrate temperature was set at 550°C. $In_xGa_{1-x}As$ was grown on a GaAs substrate. Growth rates (μm/h) are measured by the oscillation of RHEED intensity. the image of a RHEED intensity oscillation is shown in Figure 2-6, the intensity of the curve represents the surface coverage of the growing thin film. Each peak corresponds to a new monolayer formation, the layer growth rate can be obtained by measuring the oscillation frequency.

The growth rate of GaAs is kept at 1μm/h, the growth rate of $In_xGa_{1-x}As$ is changed in the range of 1.05-1.2 μm/h. With stepwise changing the In cell temperature, the growth rate of $In_xGa_{1-x}As$ is measured by the intensity oscillations of RHEED specular spot. Accordingly, the growth rate of InAs is calculated. For example, in Figure 2-6, the growth rate of $In_xGa_{1-x}As$ is 1.20 μm/h, so that the growth rate of InAs at 930°C of the In cell is 0.2μm/h. Through this process, the correct relationship between In growth rate and In cell temperature is obtained. For example, to use an In growth rate 0.08 μm/h, In cell temperature was set at 854.62°C before the re-calibration, but the appropriate temperature should be 870.92°C, as established by the new calibration. In the following experiments, the relationship between In growth rate and In cell temperature is based on the new calibration.

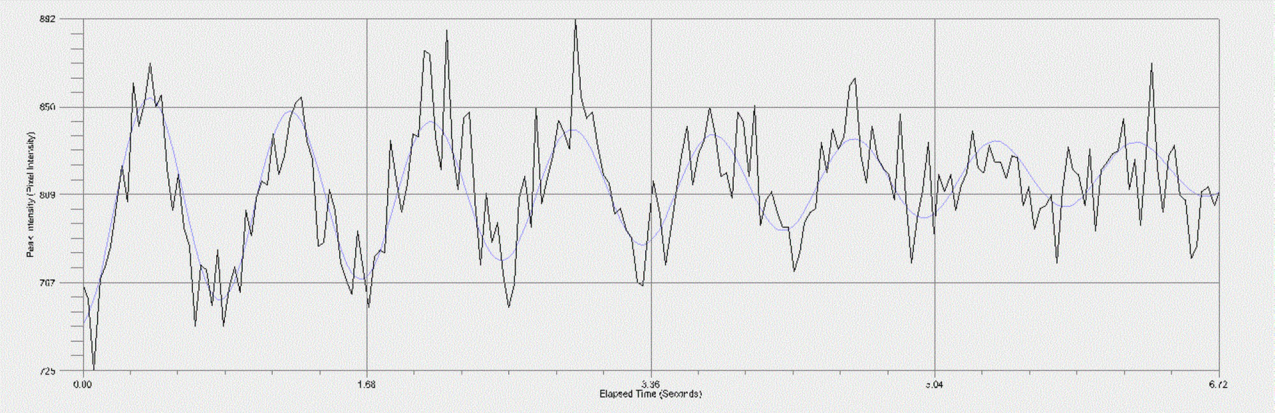
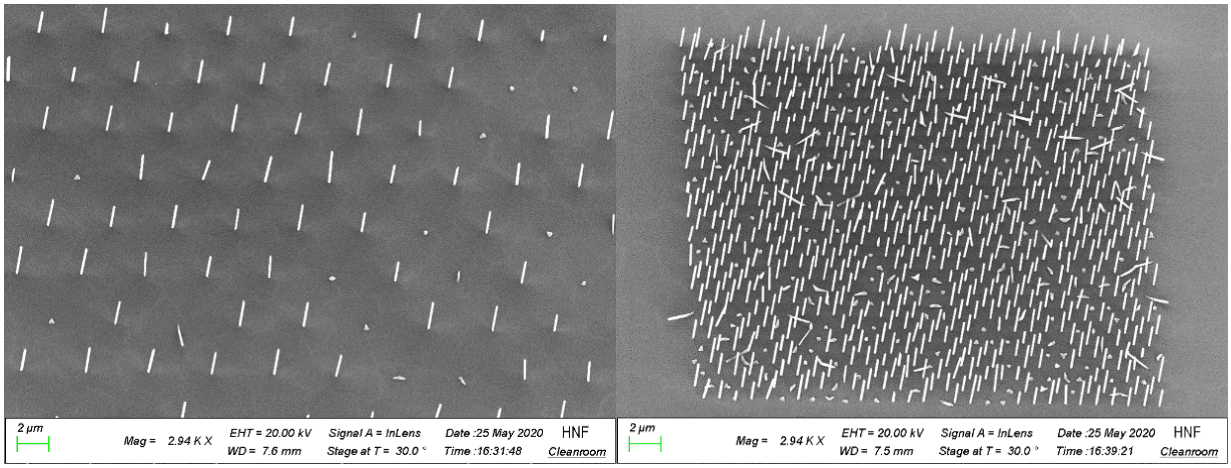


Figure 2-6. RHEED intensity oscillations during growth of $In_xGa_{1-x}As$. The x axis shows the elapsed time and y axis shows the intensity of the measured specular spot. To get this graph, In cell was set at 930°C. The growth rate of $In_xGa_{1-x}As$ is 1.20ML/s, which is equivalent to 1.20μm/h.

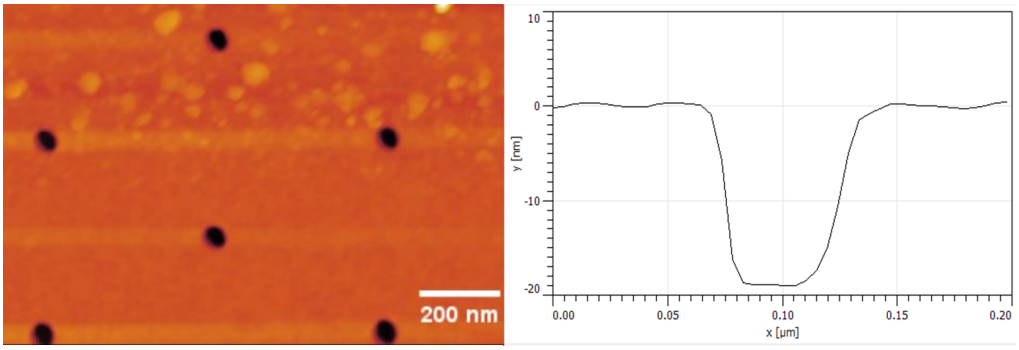
After modifying the In growth rate calibration and RIE time, the growth results have shown a higher yield of vertical nanowires, as shown in Figure 2-7. The yield of vertical nanowires can be up to 80%.



(a) (b)

Figure 2-7. SEM micrographs of a sample with RIE time 130s and new In growth rate calibration. (a) Nanowires from region D80p4 (b) nanowires from region D40P1. The growth time is 2h30min.

However, even this optimized growth method does not show high reproducibility. With the same substrate preparation parameters, the growth results are not identical from batch to batch. The reason could be that the etching rate in the RIE equipment is not stable, or that the properties of SiO_2 vary from batch to batch. One proof is that the depth of the holes after a RIE time of 110s measured two months later, is 18.75nm (evaluated from 6 holes), as shown in Figure 2-8. is almost equal to the etching depth for RIE time 140s which was measured before in Figure 2-5.



(a) (b)

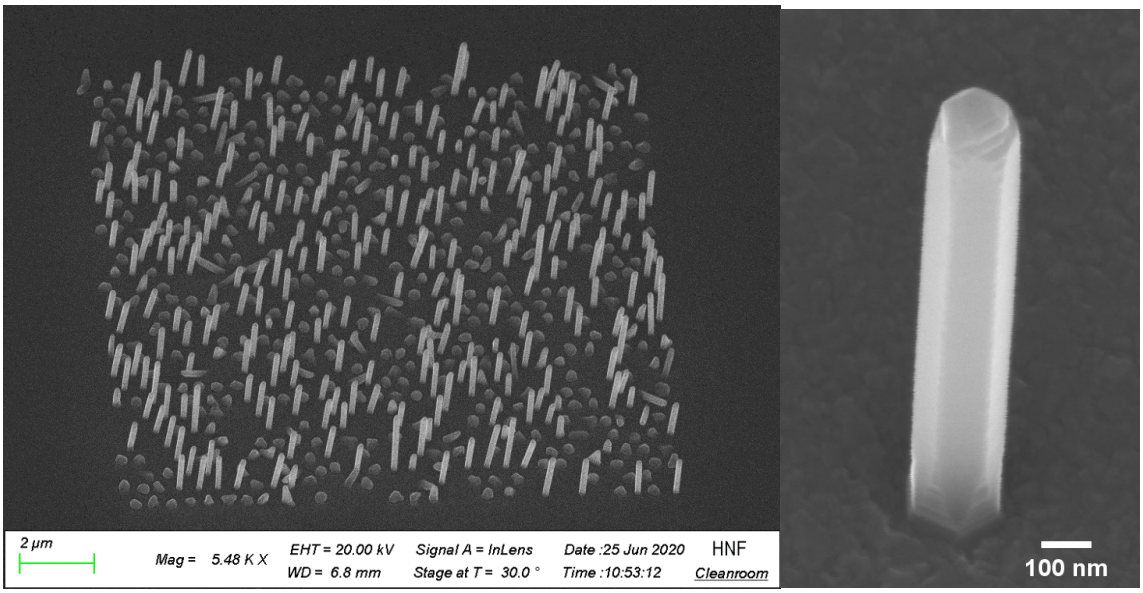
Figure 2-8. AFM measurements after 110s RIE time (details in text). (a) AFM image from region D80P500 (b) cross-sectional profile of one of the holes.

2.2 Selective growth of InAs/$Al_{0.6}Ga_{0.4}Sb$ core-shell nanowires

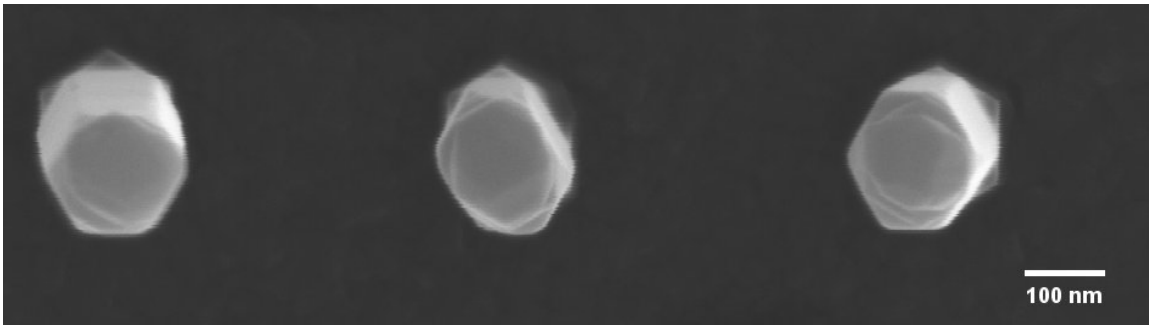
In this section, the growth, morphological and structural analyses of InAs/$Al_{0.6}Ga_{0.4}Sb$ core-shell nanowire arrays are presented. InAs/$Al_{0.6}Ga_{0.4}Sb$ core-shell nanowire heterostructure is supposed to have a staggered band alignment [33]. This structure in combination with a superconductor shell can be used for the study of the coupling of semiconductor-based quantum dot qubits.

The substrate fabrication process is the same as in section 2.1.1. In the growth process by MBE, after the growth of InAs nanowire array following the recipe described above, the In and As fluxes are stopped and the substrate temperature is reduced from 460°C to 330°C in 10min. During this time, the Sb shutter is opened and kept like this till the end of the growth. the Sb BEP is set to 1.5×10^{-6} mbar. After another 2min to stabilized the substrate temperature, the Ga and Al shutters are opened, the growth rates being set at 0.04µm/h and 0.06µm/h, respectively. After the growth of the $Al_{0.6}Ga_{0.4}Sb$ shell for a certain time, the Al shutter is closed and the Ga growth rate is set to 0.1µm/h for the growth of GaSb for 15min. According to [23], the GaSb shell growth rate is around 23nm/h, As a result, the thickness of the thin GaSb layer after 15min growth is supposed to be around 5.75nm. The thin GaSb shell prevent the fast oxidation of the $Al_{0.6}Ga_{0.4}Sb$ shell., otherwise an oxide layer of 8-10nm can be formed,, as mentioned in [22].

In order to obtain the $Al_{0.6}Ga_{0.4}Sb$ shell growth rate, shells are grown for 15min, 30min and 45min. The growth results with an AlGaSb shell growth time of 45min is shown in Figure 2-9. The growth time of the InAs core is 2h30min corresponding to a nanowire length and diameter of 2-3µm and 150-180nm, respectively. The Figures 2-9 (b) and (c) show that InAs/$Al_{0.6}Ga_{0.4}Sb$ core-shell nanowires have hexagonal morphology.

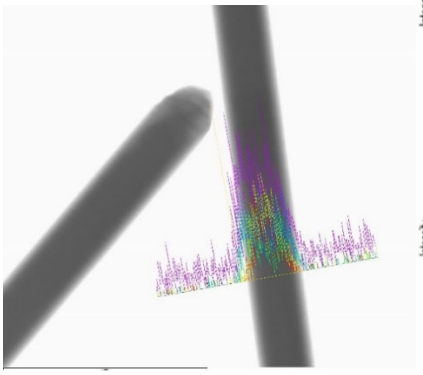


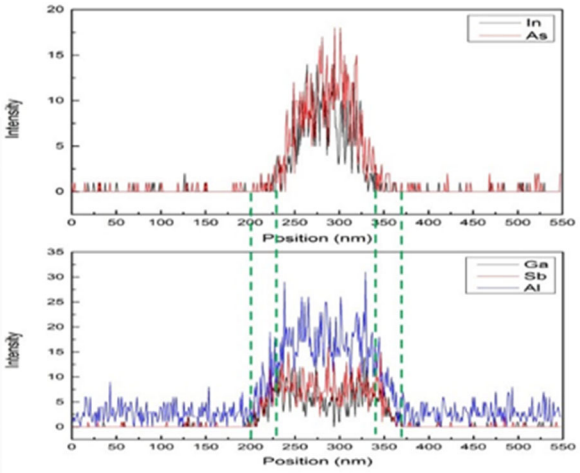
(a) (b)



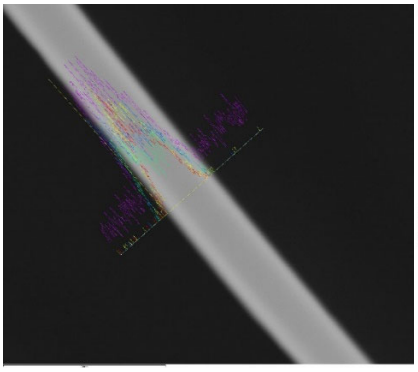
(c)

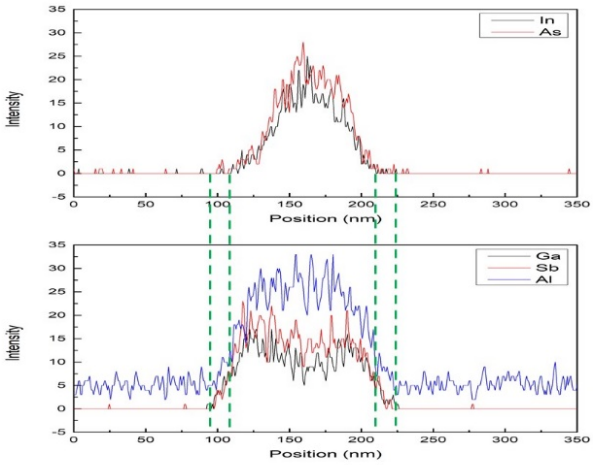
Figure 2-9. SEM micrographs of InAs/$Al_{0.6}Ga_{0.4}Sb$ core-shell nanowires with the core and shell growth time of 2h30min and 45min, respectively. (a) The 30° tilted SEM image of the array D40P500. (b) Close-up of one single nanowire (also 30° tilted SEM image). (c) Top view image of the nanowires. The nanowires with shell growth time of 30min and 15min have similar morphology except a smaller diameter.



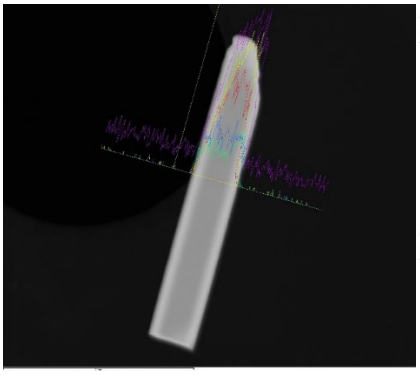

In
As
Intensity
Position (nm)
Ga
Sb
Al
Intensity
Position (nm)

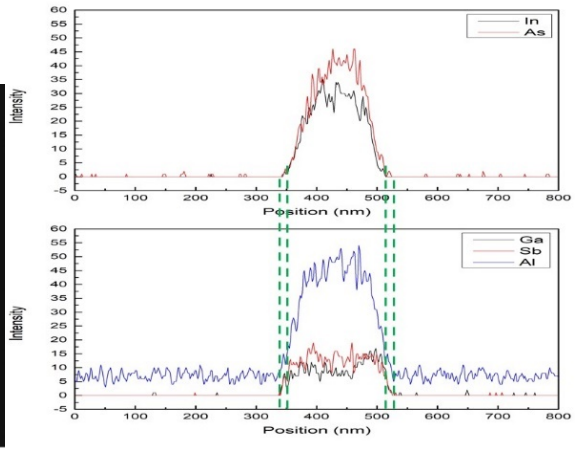
(a) (b)




In
As
Intensity
Position (nm)
Ga
Sb
Al
Intensity
Position (nm)

(c) (d)




In
As
Intensity
Position (nm)
Ga
Sb
Al
Intensity
Position (nm)

(e) (f)

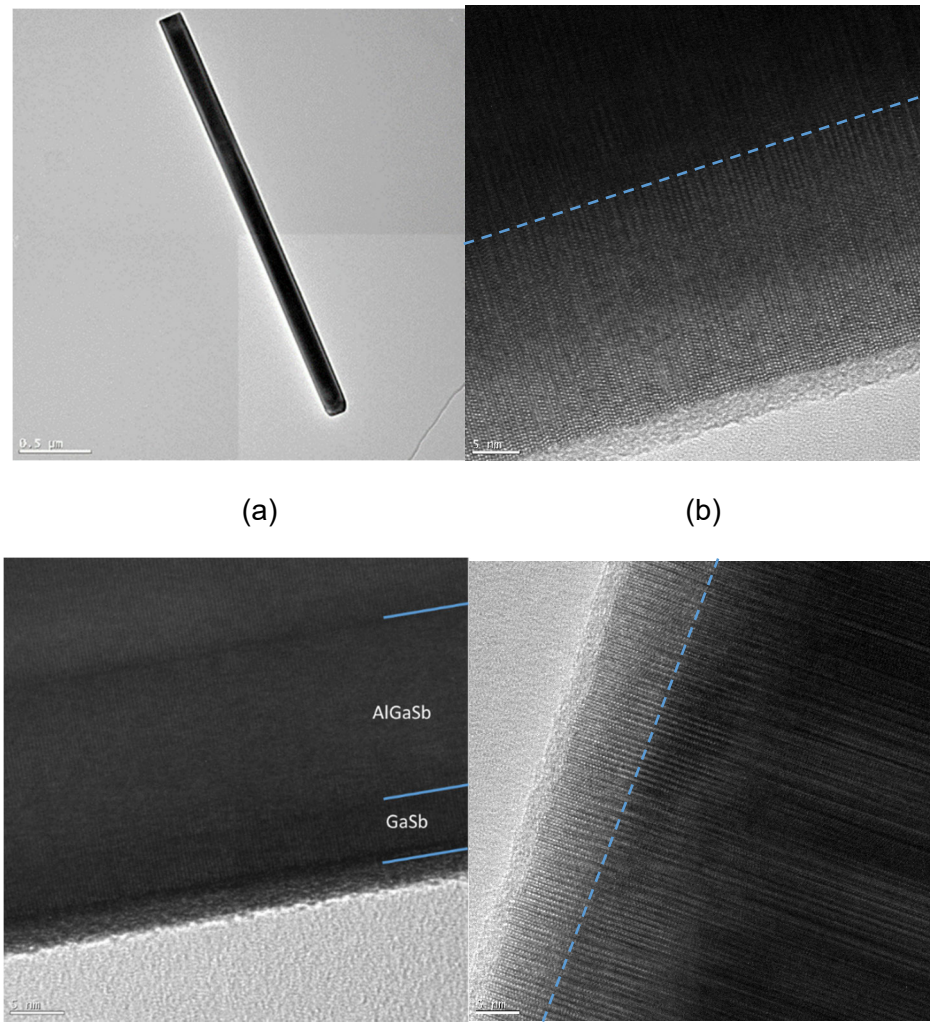
Figure 2-10. The EDX measurement of InAs/$Al_{0.6}Ga_{0.4}Sb$ core-shell nanowires with shell growth times 45min (a) and (b) , 30min (c) and (d) and 15min (e) and (f). (a)(c) and (e) show the nanowire morphology and scan lines and (b)(d)(f) show the corresponding relationship between the elemental intensity and scan position. In the lower images in (b)(d) and (f), the blue line represents Al, red line Sb and black line Ga.

In order to get the elemental distribution inside the nanowires, energy dispersive X-ray (EDX) analysis is performed. EDX is an elemental characterization method. Due to the fact that each element has a unique atomic structure, the peak on the X-ray emission spectrum is also unique and elemental information can be obtained. For measurements, the nanowires are transferred mechanically from the substrate to copper TEM grids with holey carbon films. Then, the middle part of the nanowires is scanned transversally by EDX. The results are shown in Figure 2-10. For each sample, the EDX signals of In/As and Al/Ga/Sb are shown in upper and lower images in (b)(d) and (f) respectively. The signals of In and As appear at the same position range, the signals of Al, Ga and Sb appear at a larger range than In and As, which indicate the presence of an AlGaSb shell. The intensity of In and As signal has a maximal value at the center of the core while the intensity of Al, Ga and Sb signal has a slightly decrease along the core of the nanowires.

The EDX analysis can only show the elemental composition and distribution qualitatively. The precise thickness of shell cannot be determined. Therefore, high-resolution transmission electron microscopy (HRTEM) measurements are necessary. HRTEM allows direct imaging of the crystallographic structure down to Ångström level. The method is extensively used to analyze crystal structures of semiconductors at atomic scale.

To measure the shell thickness by HRTEM, the nanowires were again transferred on TEM grids. The TEM images were taken by aligning the nanowires to the <211> zone axis or <110> zone axis of the ZB structure. Under <110> zone axis, the contrast between core and shell as well as the crystal structure of core and shell can be distinguished, while under the <211> zone axis, only the contrast between core and shell can be observed [28]. Exemplarily, the Figure 2-11 (c) is taken from <211> zone axis. The contrast between core and shell can be easily observed. The images (b) and (d) are taken from <110> zone axis and both the contrast as well as the crystal structure can be seen. A large number of stacking faults in InAs nanowires can be seen and the defects penetrating from core to shell indicates the epitaxial growth of the $Al_{0.6}Ga_{0.4}Sb$ shell. The interface between InAs and $Al_{0.6}Ga_{0.4}Sb$ is smooth and abrupt, as shown in Figure 2-11 (a). The thin GaSb cap layer can only be observed in Figure 2-11 (c) with a thickness of around 5.75nm. The

$Al_{0.6}Ga_{0.4}Sb$ shell growth time for Figure 2-11 (b), (c) and (d) are 45min, 30min and 15min, respectively. The thickness of the native oxide is 3-4nm for all TEM images. The relationship between $Al_{0.6}Ga_{0.4}Sb$ shell thickness and the corresponding growth time is shown in Figure 2-12. The $Al_{0.6}Ga_{0.4}Sb$ shell thickness is calculated by subtracting the thickness of GaSb shell (set as 5.75nm) from the total shell thickness. From Figure 2-12, a growth rate of 40nm/h for the $Al_{0.6}Ga_{0.4}Sb$ shell is obtained. This growth rate is based on the shell thicknesses of only 3-4 nanowires, the result needs to be further proven based on more nanowire data.



(a) (b)

(c) (d)

Figure 2-11. TEM images for InAs/$Al_{0.6}Ga_{0.4}Sb$ nanowires: (b) Nanowire with shell growth time 45min. a) and c) Nanowire with shell growth time 30min. d) Nanowire with shell growth time 15min.

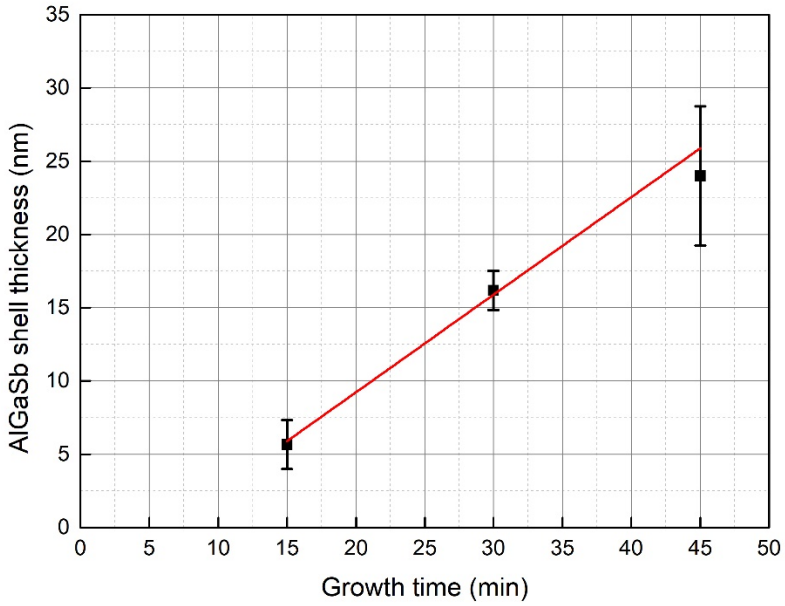


Figure 2-12. $Al_{0.6}Ga_{0.4}Sb$ shell thickness versus the corresponding growth time. The red line is the linear fit for the three different growth time.

2.3 Selective growth of InAs nanowires by MBE – new method

2.3.1 Growth mechanism

Considering the low reproducibility of the growth method introduced in section 2.1, a more stable method which is less sensitive to the substrate preparation is required. In pervious study [30], Ga pre-deposition technique has been tried for vapor-liquid-solid growth of InAs nanowires without patterning the substrate. Ga droplets create pinholes in the thin oxide which cover the Si (111) substrate as the start sites for the growth of InAs nanowires. However, the yield of InAs nanowires is low and a large amount of crystallites is achieved rather than nanowires. Recently, a high reproducible method to grow GaAs nanowires on native-SiO_x/Si(111) by using Ga pre-deposition technique was demonstrated in [34][35]. A high yield of vertical nanowires can be obtained and therefore, the method is adopted as a reference in this study. for the vapor-solid growth of InAs nanowires on prepatterned Si substrate.

In this method, a thin oxide layer is created on the Si (111) substrate followed by a surface modification procedure (SMP) before InAs nanowire growth, which consists of 3 steps:

Step 1: Surface roughening at high temperature,

Step 2: Ga droplets are deposited on the thin SiO_x layer covering the Si (111) substrate. Ga can alloy with the Si from SiO_x above a certain temperature and create small openings in the underlying SiO_x layer,

Step 3: Ga droplets are then evaporated by thermal annealing and nano holes are left behind.

In the following growth process, the nucleation of the InAs nanowires take place in the holes. The schematic of the process is shown in Figure 2-13.

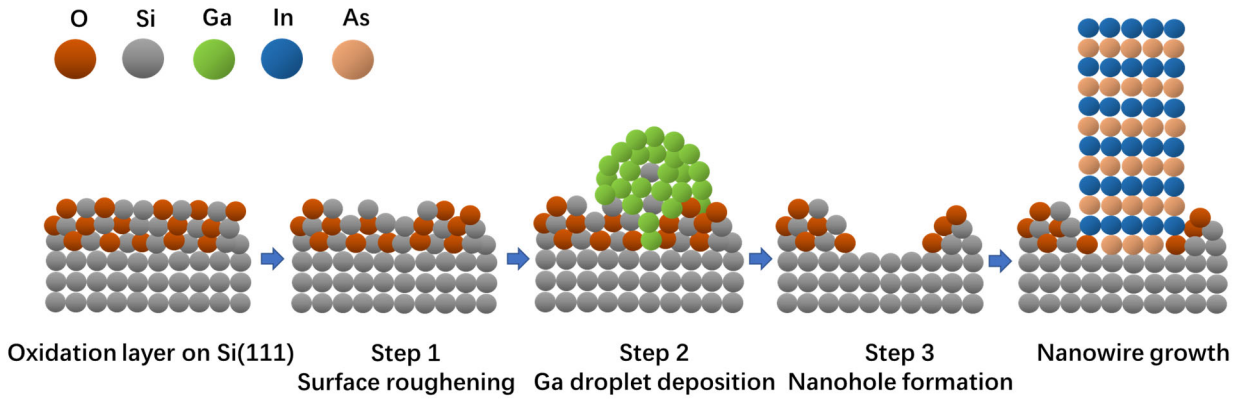


Figure 2-13. Schematic of the Ga assisted SMP of the Si(111) substrate for the InAs nanowire growth .

There are several advantages of this method, of which the highly reproducible growth results and the high yield of vertical nanowires are the two most attractive. It should be mentioned that Ga instead of In droplets are used because the solubility of Si in liquid In is very low and the pinholes cannot be created, whereas the solubility of Si in liquid Ga is much higher [36].

In this study, the precondition of the Ga droplet assisted substrate SMP is to have a thin SiO_x layer at the bottom of the patterned holes. So, the substrate preparation process needs to be modified. The ex- situ standard substrate preparation process is shown in Figure 2-14 and is as following:

The steps a)-d) are similar as presented in section 2.1.1, except that after RIE process there is no dipping into the 1% HF solution. It should be mentioned that the RIE time is 110s.

In step e) the PMMA resist is removed using acetone (6min) and isopropanol (2min). Afterwards, 10 min oxygen plasma cleaning (300W, 200sccm) at Giga batch is performed.

Then, in step f), the sample is cleaned in Piranha solution (for 10min followed by 30s etching in1% HF solution. 30s is enough to get rid of residual SiO_2 inside the hole after RIE.

The last step g) before loading the sample into the MBE system is to dip it into 37% H_2O_2 solution for 1min to re-oxidize the Si surface inside the holes. As studied in [37], the difference of the oxidation rates of hydrogen peroxide on Si (111) surface between the first and second bilayer is significant. The topmost bilayer is quickly oxidized by H_2O_2 within 30min as well as the second bilayer cannot be totally oxidized after 2 months, so that obtaining a very thin oxide layer (below 1nm) is very easily controlled. Moreover, different durations between 30s-30min of the Si (111) oxidation using H_2O_2 are investigated in [30] and 1min shows the highest density of grown InAs vertical nanowires. By using H_2O_2 substrate re-oxidation for 1min, the desired thin silicon oxide inside the holes can be obtained.

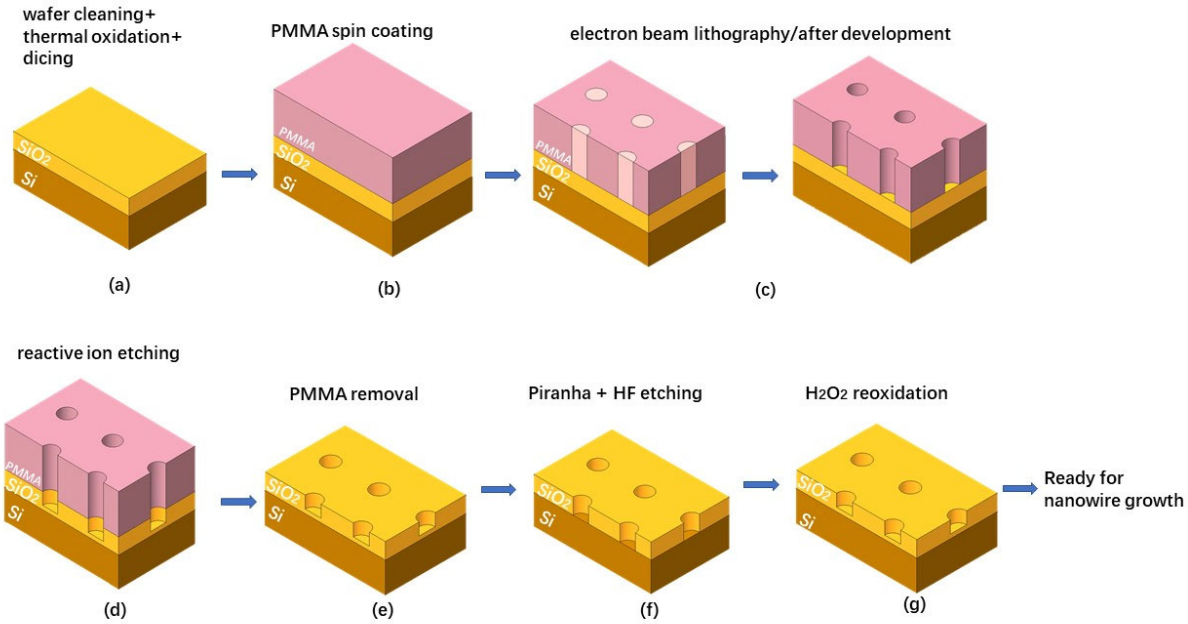


Figure 2-14. The ex-situ substrate preparation for selective growth of InAs nanowires. After step (g), there is a thin oxidation layer in the holes.

After ex-situ substrate preparation, the sample is loaded into the load lock chamber of MBE system and baked at 200°C for 45min. Then, an additional bake at 400°C for 1h is done in the preparation chamber. Finally, it is transferred into the MBE chamber for SMP and nanowire growth. The substrate temperature profile during SMP and the nanowire

growth, as well as the supplied fluxes n are shown in Figure 2-15. The SMP is conducted in the following sequence:

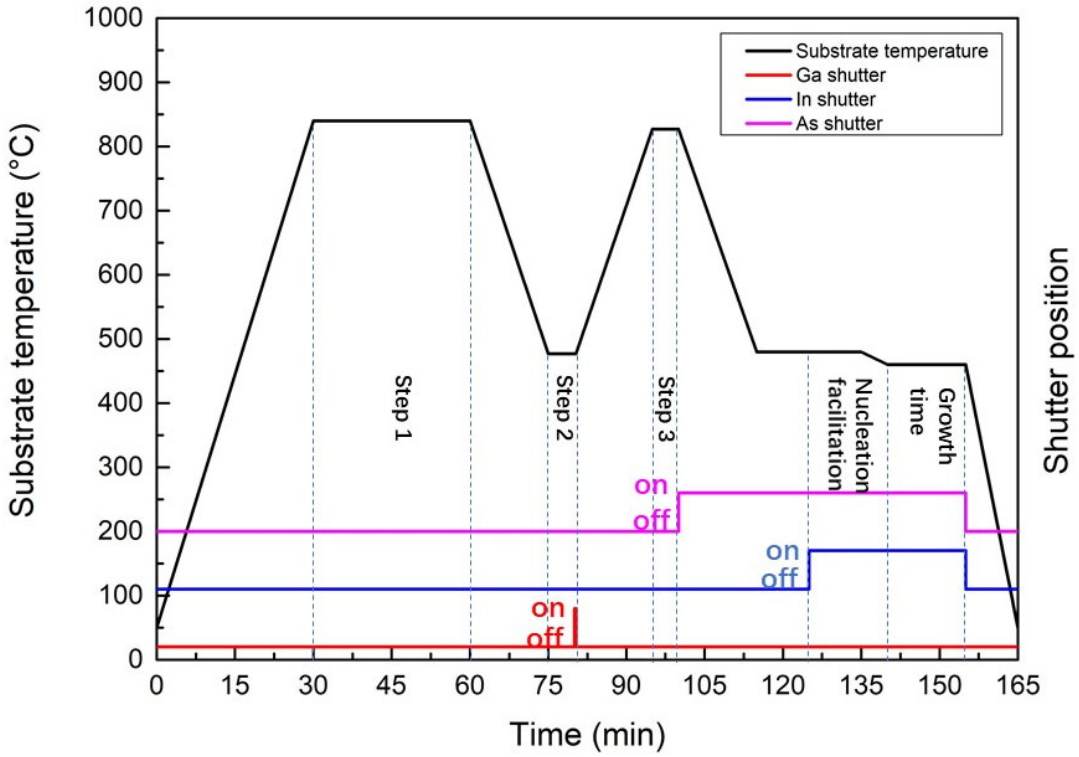


Figure 2-15. The substrate temperature profile and status of Ga/In/As fluxes during SMP and nanowire growth.

Step 1: Thermal annealing of the substrate to modify the thin SiO_2 surface inside the holes. High temperature is necessary to roughen the SiO_2 surface. This helps to have enough Ga atoms remaining on the substrate surface after Ga deposition, as discussed in [34].

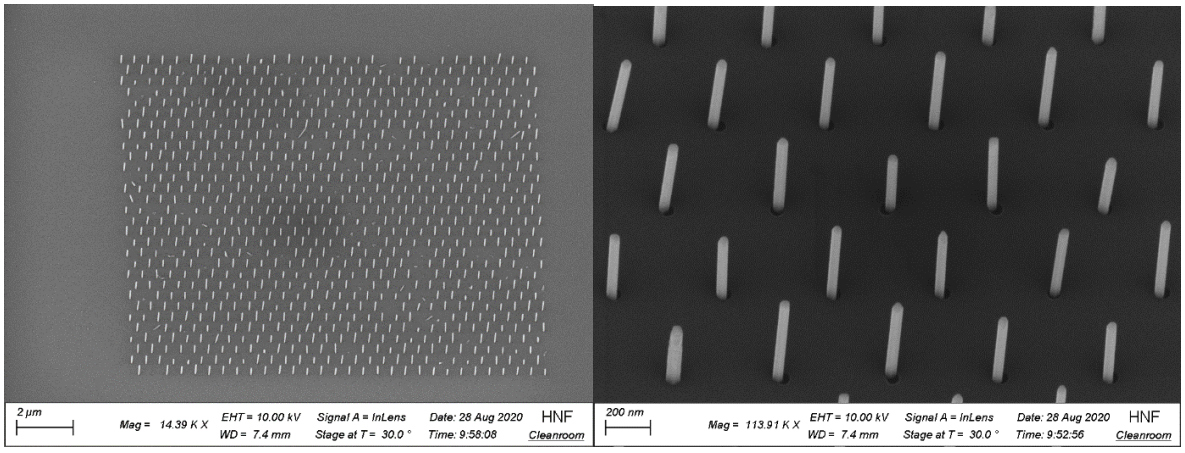
Step 2: Lowering the substrate temperature to 477°C, keep it for 5 min to stabilize the temperature and then open Ga flux with growth rate 0.16 um/h for 17.6s (the beam flux is given in equivalent growth rate of planar GaAs layer). Ga droplets are formed on the substrate surface, mainly in the holes. Because the thickness of silicon dioxide outside the holes is approximately 14nm, Ga droplets does not big enough to penetrate through. So that the openings are created only inside the holes.

Step 3: Thermal annealing of the substrate at 827°C for 5 min to evaporate Ga droplets completely and enlarge the openings. The openings are the sites where nucleation of nanowire growth takes place. Most likely, the Ga droplets are evaporated totally during the thermal annealing procedure [38] and the InAs nanowires does not contain any Ga at the bottom.

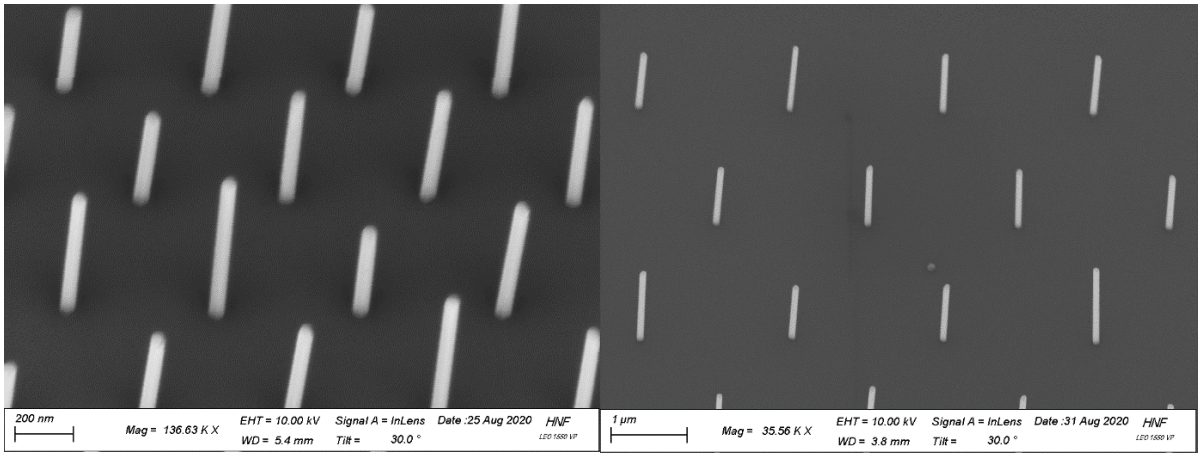
After the surface modification process, the growth procedure is the same as in section 2.1.2.: The temperature of substrate is reduced to 480°C with As flux of 4 × 10^{-5} mbar for 10min, then the In shutter is opened with flux which corresponds to a growth rate of 0.08 μm/h, while As flux remains at 4 × 10^{-5} mbar and the nanowire starts to grow for 10min. Then, the substrate temperature is reduced to 460°C in 5 min and simultaneously the In rate is reduced to 0.03 μm/h and As BEP is reduced to 2.5 × 10^{-5} mbar. This growth conditions are maintained until the end of the growth and the corresponding time is defined as the growth time.

2.3.2 Growth results and analysis

The growth result after the standard substrate preparation and growth process is shown in Figure 2-16. In the areas with hole diameter 20nm and 40nm, a very high density of vertical nanowires with very few crystallites or tilted nanowires is clearly observed.



(a) (b)



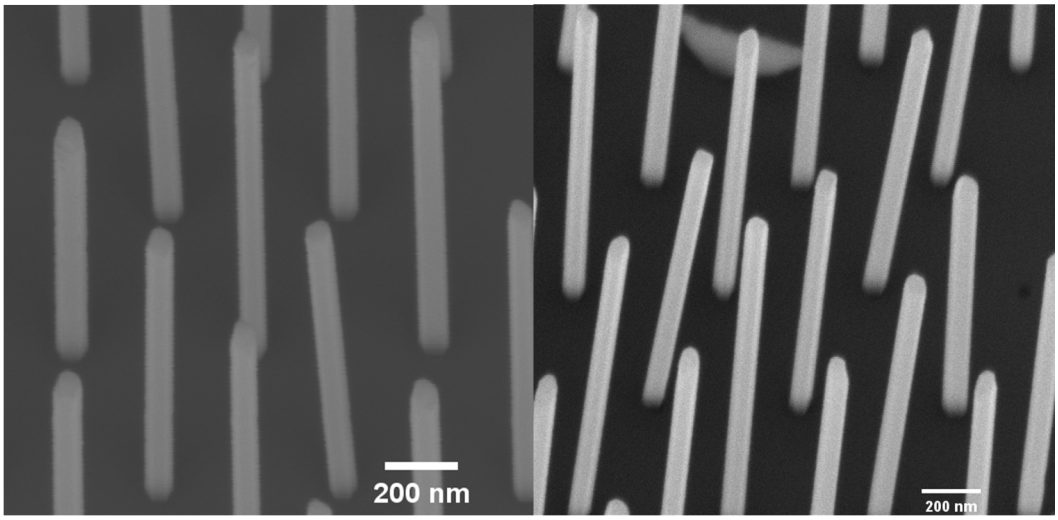
(c) (d)

Figure 2-16 30° tilted SEM images from InAs nanowire arrays grown with new substrate preparation method: (a) Overview of a nanowire array in the area D40P500 with growth time 15min. (b) Close-up of several nanowires in (a). (c) Area D20P500 with growth time 30min. (d) Area D40P2 with growth time 1h.

2.3.3 The influence of different substrate preparation processes

The nanowire growth presented in section 2.1 is very sensitive to substrate treatment. So, it is necessary to know how changes in the ex-situ substrate preparation influence the new nanowire growth method.

The growth results with 110s RIE process and 20s HF solution immersion, and the growth results with 130s RIE process and totally 120s HF solution immersion are shown in Figure 2-17. Both samples show similar growth results regarding the nanowire length, diameter and the yield. Thus, the HF immersion time can be reduced to 30s with no doubt. Based on the same experiments one can say that the growth is also not sensitive to the RIE time. We can conclude that the new substrate preparation method using Ga droplets gives more reliable and stable growth results than the method presented in section 2.1.

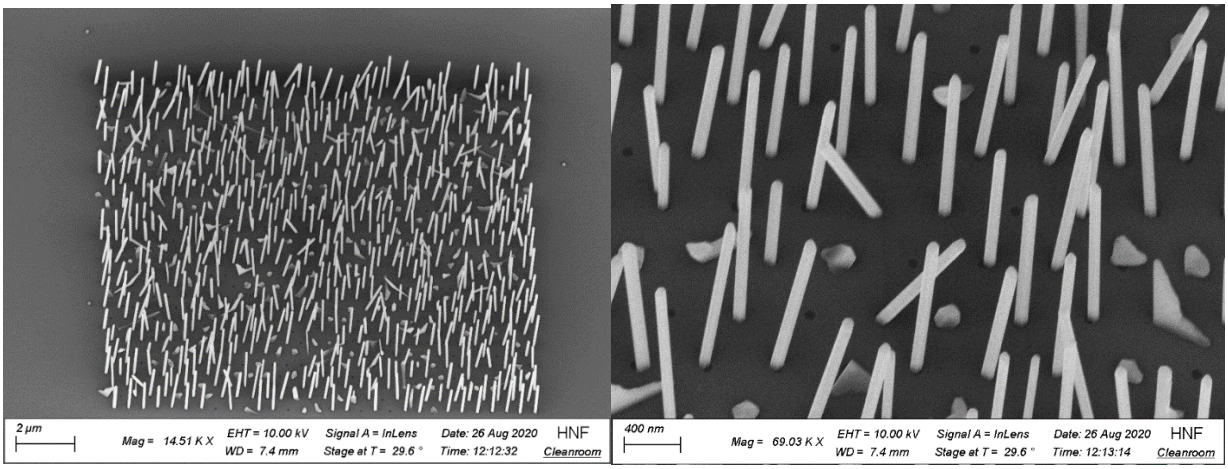


(a) (b)

Figure 2-17. Comparison of different ex-situ substrate preparation. (a) substrate processed with 110s RIE etching and 20s HF dipping. (b) substrate processed with 130s RIE etching and 60s HF dipping directly after RIE process plus 60s HF solution dipping after cleaning with Piranha solution. Both images are with growth time 1h30min from area D20P500.

2.3.4 The influence of different substrate re-oxidation before MBE growth

In the standard substrate preparation, 37% H_2O_2 solution is used to re-oxidize the Si surface inside the holes. It is known that Si substrate can also be oxidized by storing in the air for certain time resulting in a thin layer of native oxide. As reported in [39], for Si(111) substrate at atmospheric humidity 40%, the thickness of native oxide remains at around 0.7nm-0.8nm for a storing time longer than 1 week. For comparison, one sample was stored in the air in the cleanroom for 1 week and afterwards, it was grown under the standard growth condition. The result is shown in Figure 2-18. It can be observed clearly that the growth result is worse than on the substrate with H_2O_2 treatment as shown in Figure 2-17 (a) and (b). There are more empty holes, tilted nanowires and crystallites.

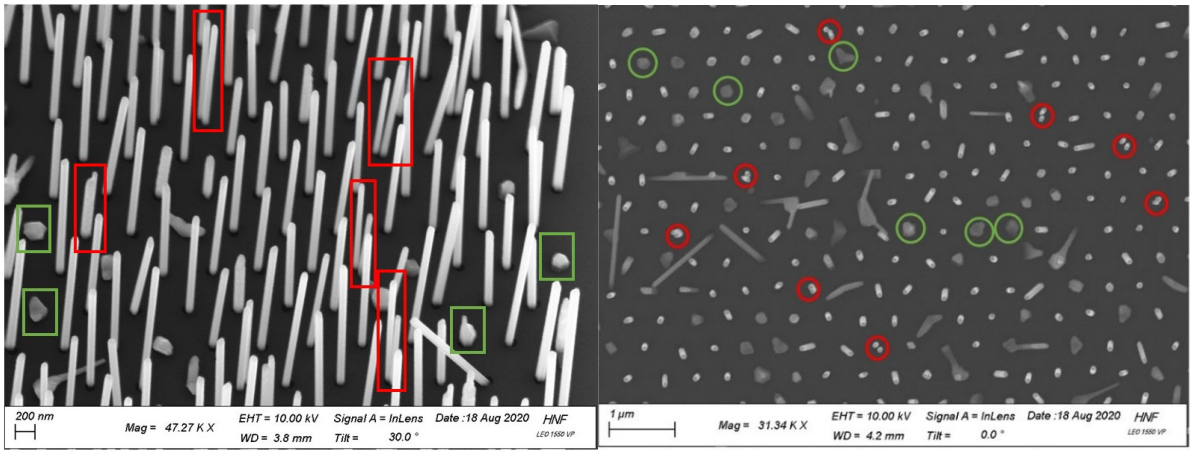


(a) (b)

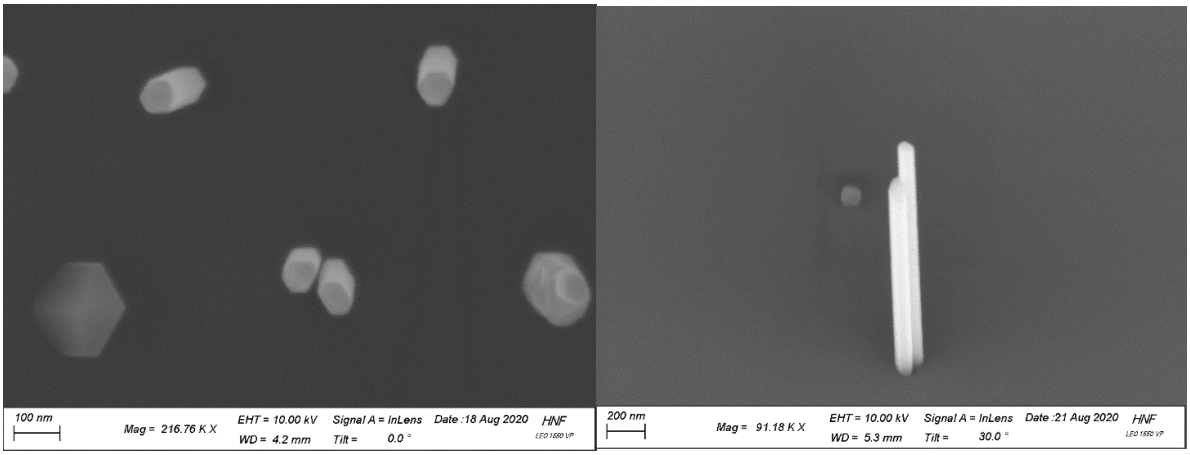
Figure 2-18 30° tilted SEM image of the nanowire array D40P500. The growth time is 1h30min and the substrate is re-oxidized in the air before loading into MBE (a) Overview of the nanowire array. (b) Close-up of several nanowires.

2.3.5 The influence of different hole diameters

The images above are all from arrays with hole diameters 20nm or 40nm. Basically, from one hole only one nanowire grows. But for larger hole diameters 60nm and 80nm, two nanowires can grow from one hole, as shown in Figure 2-19. (a) and (b) shows the overview of nanowire array with D60P500. The twin nanowires are marked with red frames (circles) and the crystallites are marked with green frames (circles). Images (c) and (d) displays the twin nanowires with higher magnification. The nanowires have an irregular hexagonal morphology, as indicated in image (c).

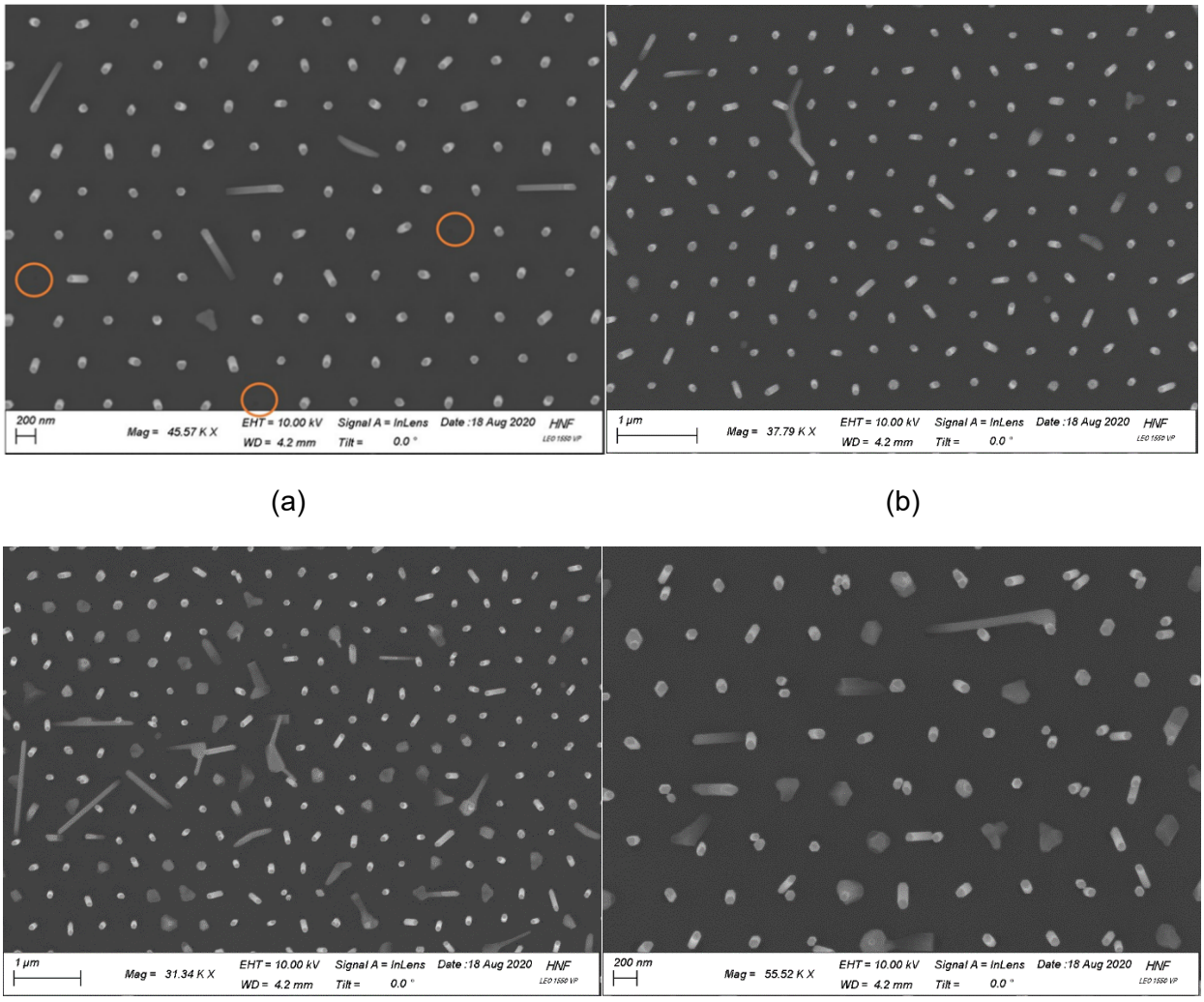


(a) (b)



(c) (d)

Figure 2-19 (a) 30° tilted SEM image from the array D60P500 (b) Top view SEM image from the same array. (c) Top view of nanowires with higher magnification. (d) Close-up of twin nanowires.



(a) (b)

(c) (d)

Figure 2-20. The top view of SEM images from the arrays (a) D20P500 (b) D40P500 (c) D60P500 and (d) D80P500. The growth time of this sample is 1h30min. In image (d) it appears that even three nanowires can grow from one hole, as shown in the fourth hole position in the first line.

As displayed in Figure 2-20, the yield of vertical nanowires shows hole diameter dependence. With increasing hole diameter, the number of twin nanowires, tilted nanowires and crystallites increases. The yield of nanowires (defined as the ratio between normal single vertical nanowires and all the other structures) function of hole diameters is shown in black in the Figure 2-21. It is obviously that with increasing hole diameter, the yield decreases while the percent of twin nanowires and crystallites/inclined nanowires increases. The yield of nanowires in the array D20P500 is 94% while in the array D40P500 is 88%. It should be mentioned that when the diameter is 20nm, there are a few empty holes, as shown in orange circles in Figure 2-20 (a), which doesn't show up for

larger hole diameters. Overall, the arrays with hole diameters 20nm and 40nm have the best results. Therefore, the electrical measurements in chapter 5 are based on the arrays with hole diameters of 20nm and 40nm.

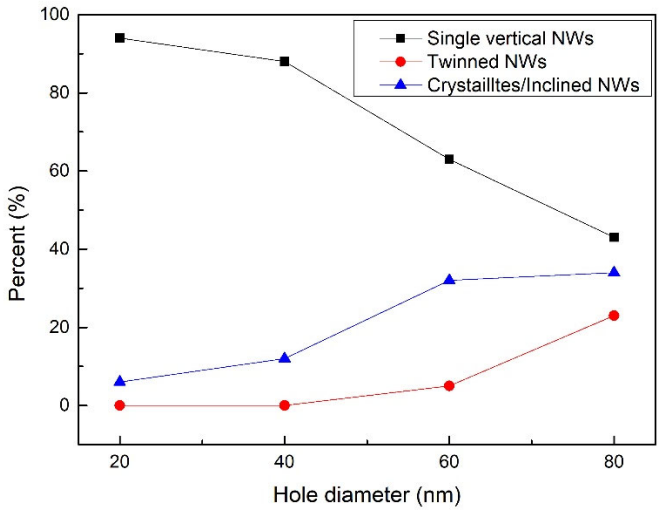


Figure 2-21. The relationship between hole diameters and the percent of normal single vertical NWs, twin nanowires, as well as tilted nanowires and crystallites.

The reason for the twin nanowires in one hole could be that holes with larger diameters provide a larger area to accept the depositing of more Ga droplets in the pre-deposition step. As reported in [34], the Ga droplets exhibit diameters in the range of 16-25nm and height in the range of 8-12nm, and the pinhole in the thin oxide layer under the vertical nanowires is approximately 5-8 nm in diameter. Therefore, for hole diameters 20nm and 40nm, only one droplet deposits inside the hole, but for hole diameters 60nm or 80nm, it is possible that two droplets (or even three droplets for 80nm) deposit inside the hole, react with the SiO_x thin layer separately and create openings separately, which results in more than one nucleating sites inside the hole, therefore more than one nanowire can grow from one hole.

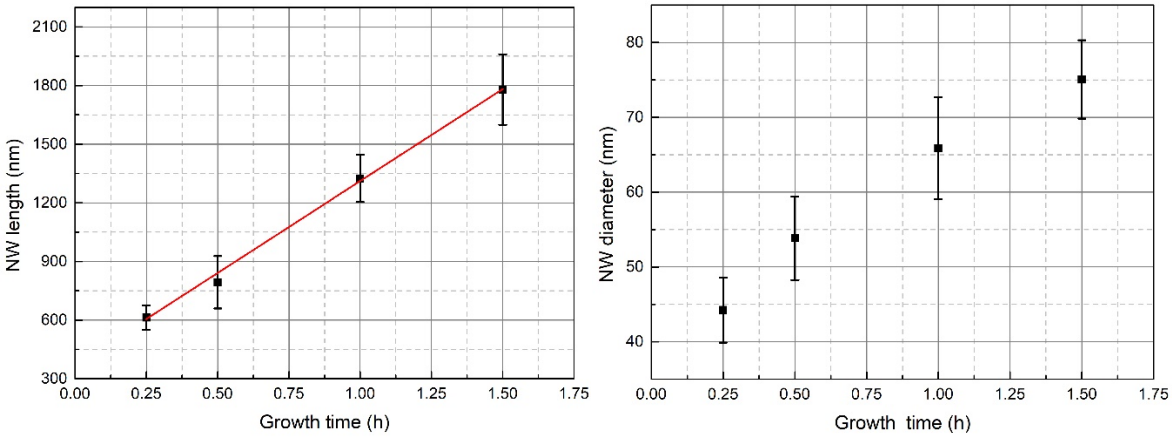
2.3.6 The influence of growth time and different pitches

As shown in Figure 2-22 (a), with increasing growth time, the length of nanowires increases almost linearly. The equation of the fitting line is

$$y=371+940x \text{ (with coefficient of determination } R^2=0.996)$$

The y-axis intercept indicates that the nanowires has already an average length of 371nm after the nucleation facilitation time. The growth rate is approximately 940 nm/h.

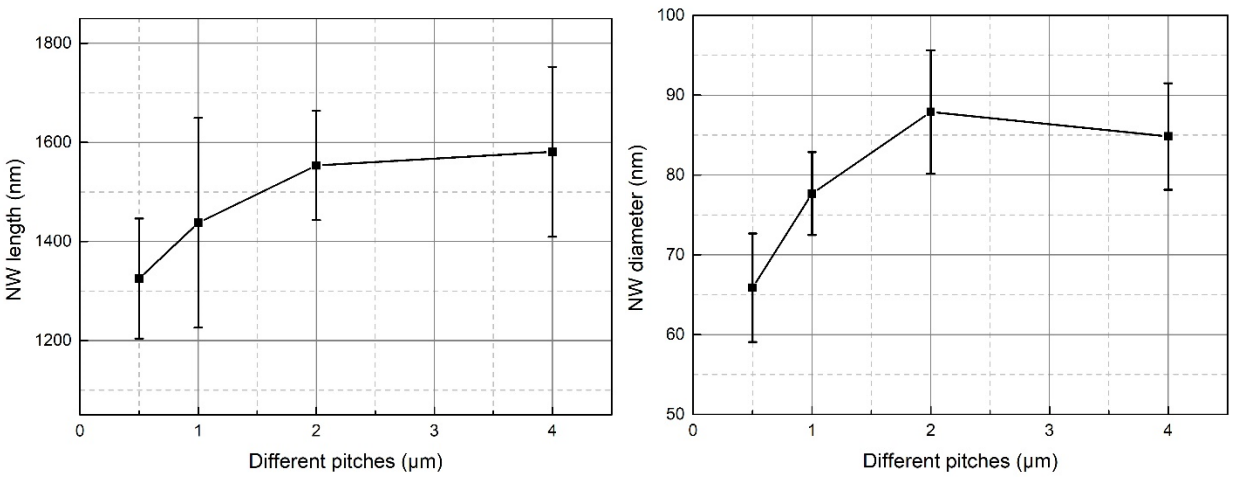
As plotted in Figure 2-22 (b), the nanowire diameter increases with time faster at the beginning and slightly slower later.



(a) (b)

Figure 2-22. The relationship between nanowire length/diameter and growth time. These data are based on the measurement of 10 nanowires from array D40P500 from each sample. The error-bars represent the standard deviation of the ten measurements.

In Figure 2-23 the nanowire length and diameter are plotted function of the pitches. As seen, the nanowire length and the nanowire diameter increase with increasing pitches from 500 nm to 2 μm, but for pitch 2 μm and 4 μm, the nanowire length keeps almost constant, the diameter can even decrease. This trend is the same as shown in [28]: below 2μm pitch the growth is in competitive growth regime, the growth rate increases as the capture area for surface diffusing In adatoms per nanowire increases. Above 2 μm pitch, the growth is in diffusion limited regime, the pitch is larger than twice of the diffusion length of In adatoms and therefore the growth is limited by the diffusion length of In adatoms. The deviation amount of nanowire length and diameter is irregular with increasing pitches.



(a) (b)

Figure 2-23. The relationship between nanowire length/diameter and pitches. These data are based on the measurement of 10 nanowires for each pitch from an array D40P500 with growth time 1h.

3. Passivation of InAs nanowire by ALD

In order to investigate the influence of the dielectric passivation on the electrical properties of the InAs nanowires, in-situ atomic layer deposition (ALD) is used to grow an Al_2O_3 shell. In the ALD chamber, the reaction between the precursor trimethylaluminum (TMA, $Al(CH_3)_3$) and the co-reactant H_2O occurs at 250°C. After 125 cycles around 10nm thick Al_2O_3 shell is deposited on the InAs nanowires.

After the growth of InAs nanowires in the MBE chamber, the sample needs to be transferred to ALD chamber without taking it out from the ultrahigh vacuum. During the MBE growth, the substrate is upside down. On the contrary, the substrate is right side up during ALD growth. In this situation, a pocket wafer and flipping ring are needed in order to flip the substrate 180° before to be introduced in the ALD chamber. The flipping ring is thicker than the normal ring.

As mentioned in section 2.1.2, the substrate temperature in the MBE system is measured by a thermocouple. The thermocouple is situated closely above the sample, as shown in Figure 3-1. But due to the thermal obstruction of the pocket wafer between thermocouple and substrate and the different ring, the same temperature measured by the thermocouple correspond to a real temperature of the substrate different from the real temperature when using the normal ring.

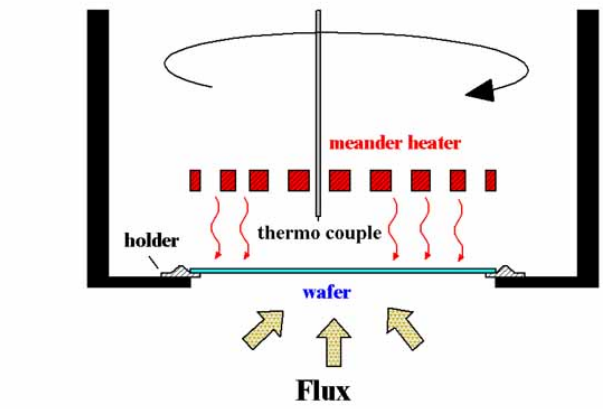


Figure 3-1. Schematic of the substrate, substrate holder and substrate heater during growth. [40]

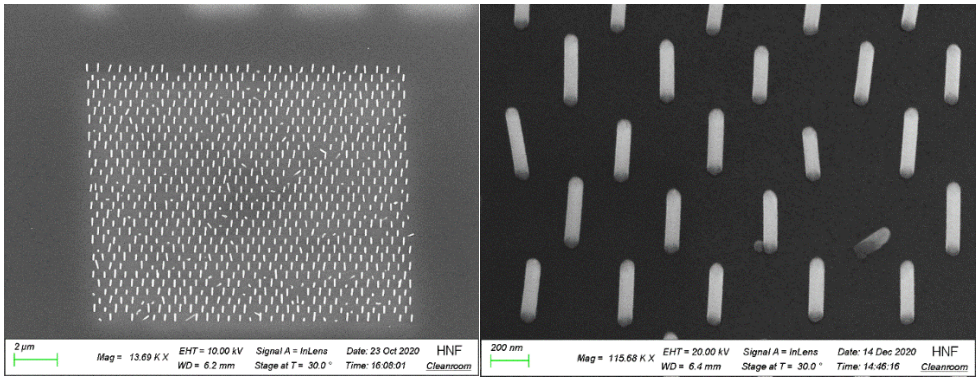
To set the substrate temperature during growth correctly, the real temperature of substrate during growth needs to be measured. The real temperature measurement is

based on emissivity corrected pyrometry. The pyrometer is located at the bottom of the chamber. It is a remote-sensing thermometer, which uses the amount of thermal radiation emitted from objects to determine their temperature. The emissivity can be corrected using the reflectance measured in the same time.

First, a sample was grown with the normal ring and the real temperature of the substrate during the whole growth process was recorded. The real temperature is usually lower than that measured by the thermocouple, as shown in Table 3-1. Afterwards, another substrate was grown with flipping ring and pocket wafer. During the growth, the same real substrate temperatures have been used and the new corresponding thermocouple temperatures have been recorded. The correspondence between the thermocouple temperature and the real temperature is shown also in Table 3-1. Figure 3-2 shows an array of Al_2O_3 passivated nanowires using for the MBE growth the temperature calibration of the flipping ring. The nanowires are grown successfully, which indicates the correct growth temperature.

Table 3-1 The growth temperature calibration for normal and flipping ring

Normal ring		Flipping ring with pocket wafer	
$T_{thermocouple}$/°C	$T_{pyrometer}$/°C	$T_{thermocouple}$/°C	$T_{pyrometer}$/°C
840	760	985	760
477	455	574	455
827	750	975	750
480	458	578	458
460	425	558	425



(a) (b)

Figure 3-2. The morphology of Al_2O_3 passivated InAs nanowires grown with the flipping ring with nanowire growth time 15min and 10nm Al_2O_3 passivation (array D20P500).

4. InAs nanowire-array based device fabrication

The usual pick and place approach for nanowire device fabrication which involves only one single nanowire is very time consuming, and needs high requirements for the lithography. Therefore, InAs nanowire-array based devices are fabricated in this thesis, in order to measure the electrical characteristics of nanowires and to investigate the influence of passivation.

The schematic of the device architecture is shown in Figure 4-1. Each nanowire array as a whole is connected by a top electrode and the bottom electrode is directly deposited on the highly n-doped Si substrate. The electrical characteristic can be achieved by connecting metallic probes on top and bottom electrodes. To achieve this device architecture, the following 4 steps are performed. The detailed description is shown afterwards.

1. Dicing of the 2.5*2.5 cm^2 substrate
2. Planarization the samples with HSQ
3. Revealing the top of nanowires
4. Top/bottom electrode fabrication

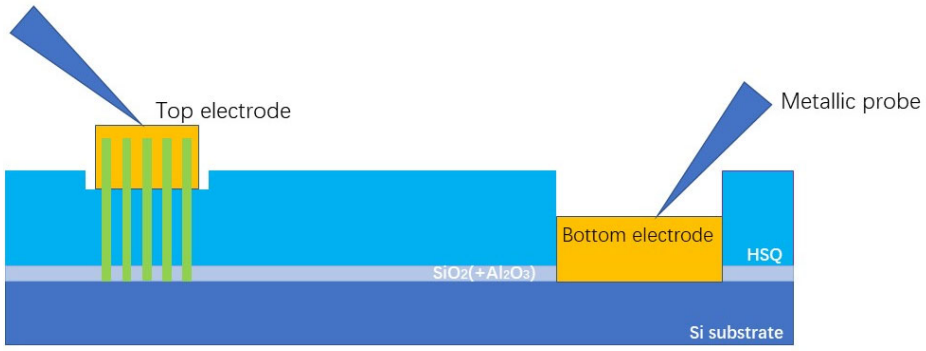
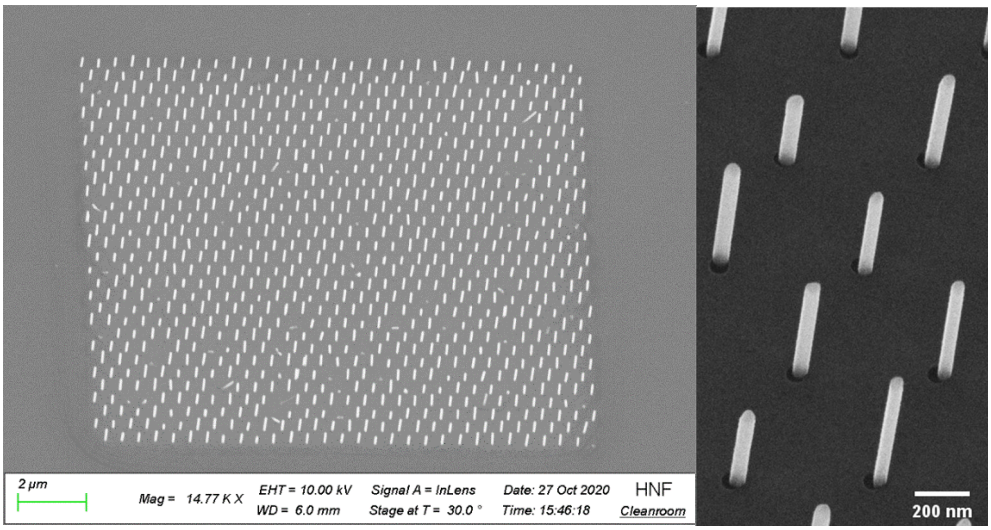
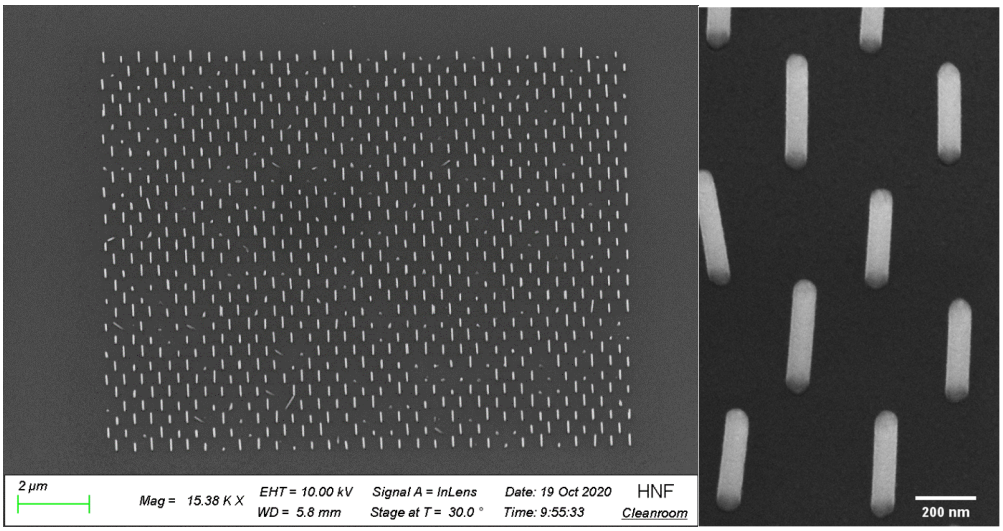


Figure 4-1. The schematic of the device architecture.

The fabrication is done using a sample with InAs nanowires and one with Al_2O_3 passivated InAs nanowires. They are both with 15min nanowire growth time and the thickness of the Al_2O_3 shell for passivated nanowires is around 10nm. Exemplarily, SEM images of a nanowire array from both samples are shown in Figure 4-2. Comparing (b) and (d), it is obviously that the diameter of the nanowires in (d) is larger than in (b), which indicates the presence of Al_2O_3 shell.



(a) (b)



(a) (d)

Figure 4-2. SEM micrographs of the samples used for the device fabrication. (a) and (b) Nanowire morphology of the array D40P500from the sample with InAs nanowires. (c) and (d) Nanowire morphology ofthe array D40P500 from the sample with Al_2O_3 passivated InAs nanowires.

4.1 Dicing

First, after the growth, the 2.5*2.5 cm^2 substrates was spin-coated with resist AZ5214E at 500rpm for 30s which was baked at 90°C for 3min. Afterwards, they were diced into 4 pieces each with the size 1.25x1.25cm^2. The spin-coating speed was low because the nanowires are fragile and at high speed there is the risk to brake or bend. After dicing,

the substrates were cleaned with acetone and isopropanol without using ultrasonic bath because even 1 min in the bath at the lowest power will lead to the break of most of the vertical nanowires from the Si substrate. The processes mentioned bellow were all performed on these pieces with sample size 1.25x1.25cm^2.

4.2 Planarization with HSQ

Prior to the fabrication of the top and bottom contacts, it is necessary to planarize the substrate surface. The polymer hydrogen silsesquioxane (HSQ) is used in this study as the planarization material. HSQ exhibits a good gap fill capability and low dielectric constant (k <3.0). Therefore, it is a potential candidate for the formation of interlayer dielectrics to enhance the performance of integrated circuits. HSQ is commercially available in a carrier solvent of methyl isobutyl ketone (MIBK). The fluidity of HSQ makes the spin-coating process possible and the layer can serve as an isolating and supporting material between top and bottom electrode. It can also work as negative inorganic electron beam resist with high resolution [41].

HSQ polymers consist of three-dimensional molecules with chemical composition $(HSiO_{3/2})_n$. A representative molecular structure is illustrated in Figure 4-3 (a). HSQ has a mixed cage-network structure before curing and transforms from cage-network structure to network structure after curing, as seen in Figure 4-3 (b). During curing process, Si-H bonds disassociate, molecules rearrange and O-Si-O bonds form [42][43]. then HSQ turns into a material with similar chemical composition as SiO_2.

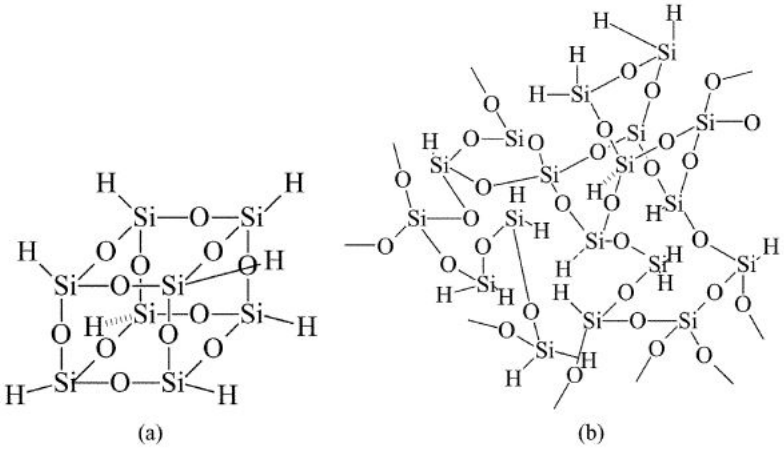


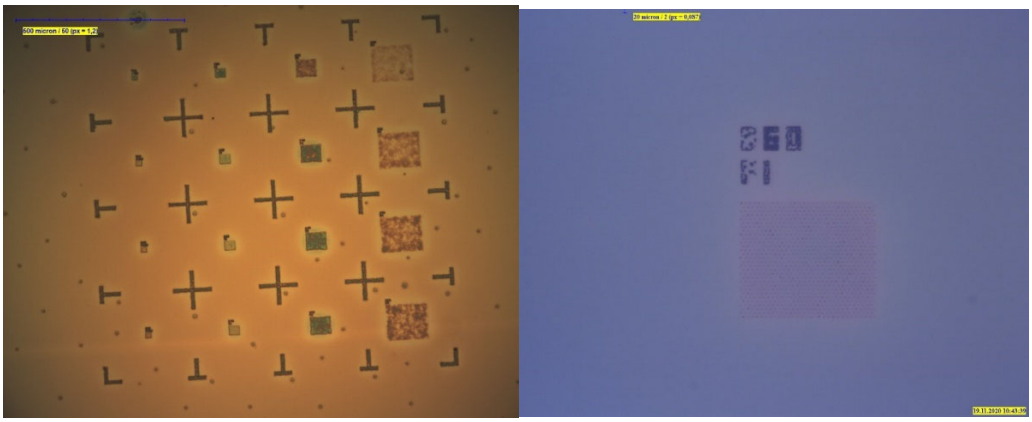
Figure 4-3. (a) Cage structure of HSQ. (b) Network structure of HSQ. Taken from[44].

In the spin-coating process, the entire sample surface was covered with the HSQ solution and was left to stand for 2 min to ensure the filling of the narrow gap between the

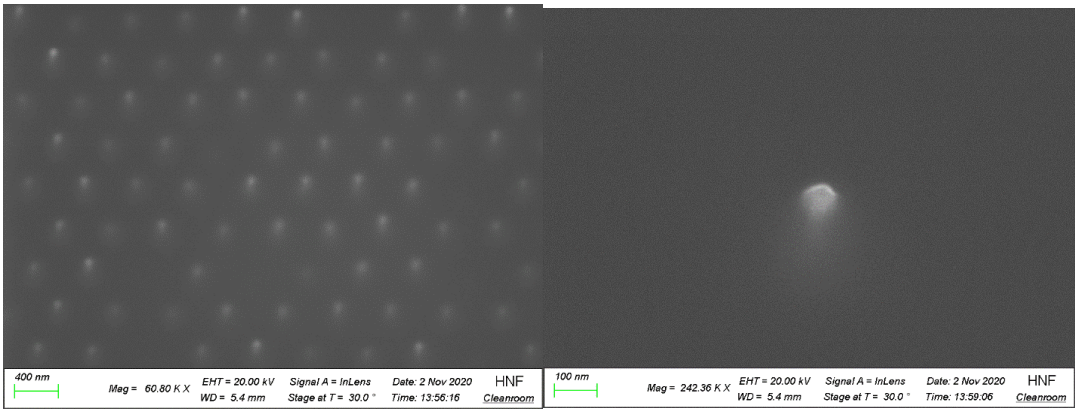
nanowires. Afterwards, it was spun at 1000 rpm for 1 min (acceleration 200 rpm/s), and then baked on the hot plate at 150°C for 2min and at 220°C for 5min in order to remove the solvent and initiate structural changes. Then the sample was transferred into rapid thermal processing (RTP) equipment to cure the HSQ layer at 300°C for 15min in N_2 atmosphere. After this process, the HSQ structure was modified into an amorphous silica structure.

The thickness of HSQ was measured by Ellipsometer SE800. The thickness of one layer of HSQ under the above condition is 200±10 nm. The length of InAs nanowires with growth time 15min is around 600 nm. As a result, three layers of HSQ are required to planarize the nanowires. The spin-coating and RTP processes were repeated three times and around 600nm of dielectric layer was achieved after planarization.

The Figure 4-4 shows images during the planarization of nanowires without passivation. Figure 4-4 (c) shows the most of the nanowires are totally covered by HSQ. For sample with Al_2O_3 passivation, similar results were obtained.



(a) (b)



(c) (d)

Figure 4-4. Optical microscope (a) and (b) and SEM (c) and (d) images from the sample with InAs nanowires without Al_2O_3 passivation. (a) After 1 layer of HSQ spin-coating. (b) After 3 layers of HSQ planarization. (b) Array D40P500 after 3 layers of HSQ planarization. (d) Close-up of a nanowire top.

4.3 Revealing the top of nanowires

After the planarization process, the next step is to etch back the HSQ layer using RIE by CHF_3 in order to reveal the top of nanowires. The etching rate of HSQ in the RIE process using CHF_3 is around 0.28nm/s, as shown in Figure 4-5. 5min RIE is performed for both samples with and without passivation. After the RIE process, around 84nm HSQ is etched. Exemplarily, SEM images of both unpassivated and passivated nanowire areas are shown in Figure 4-6 and Figure 4-7, respectively.

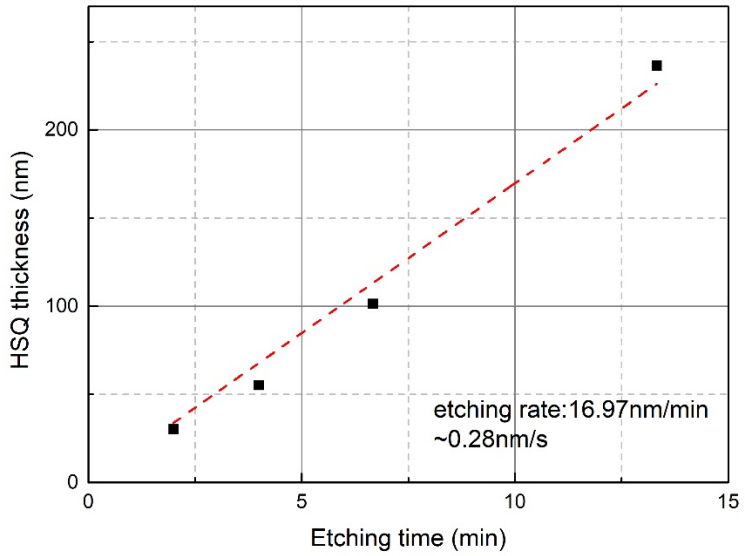
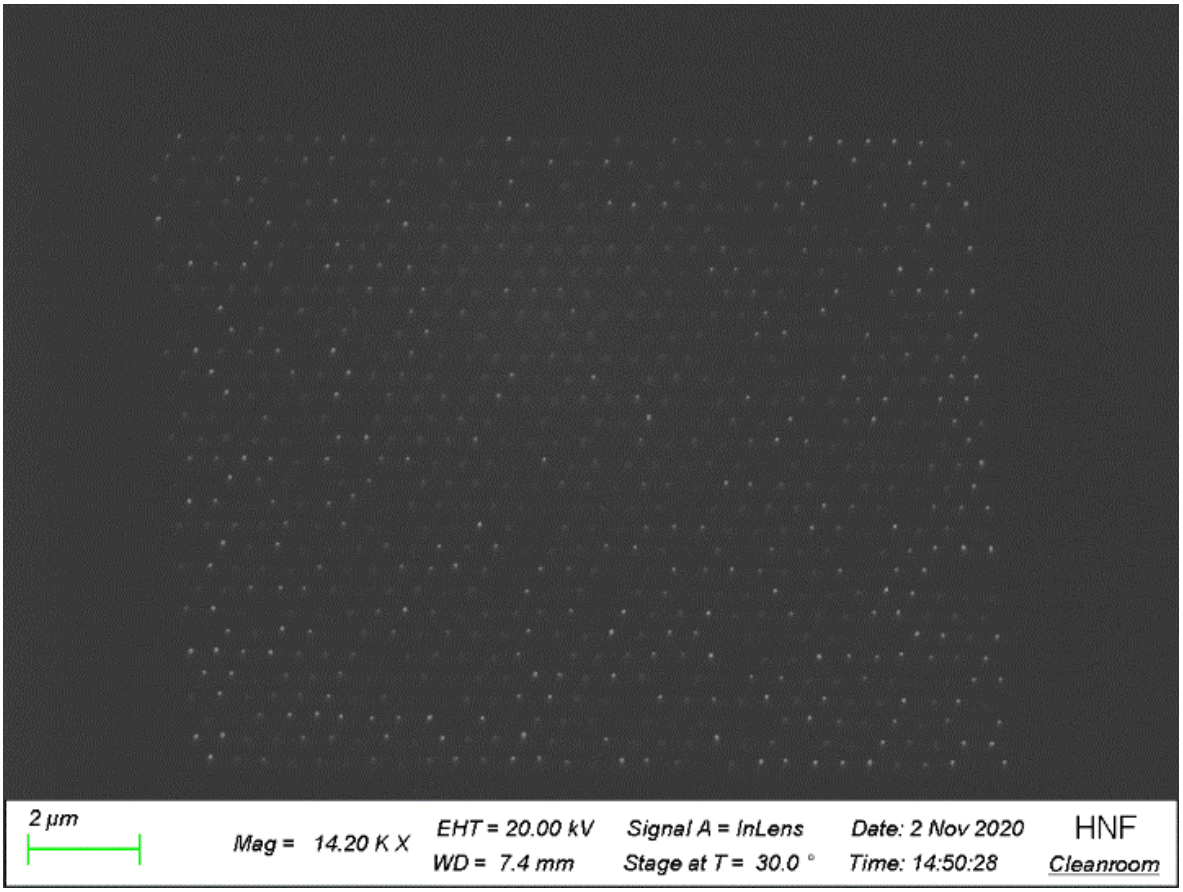
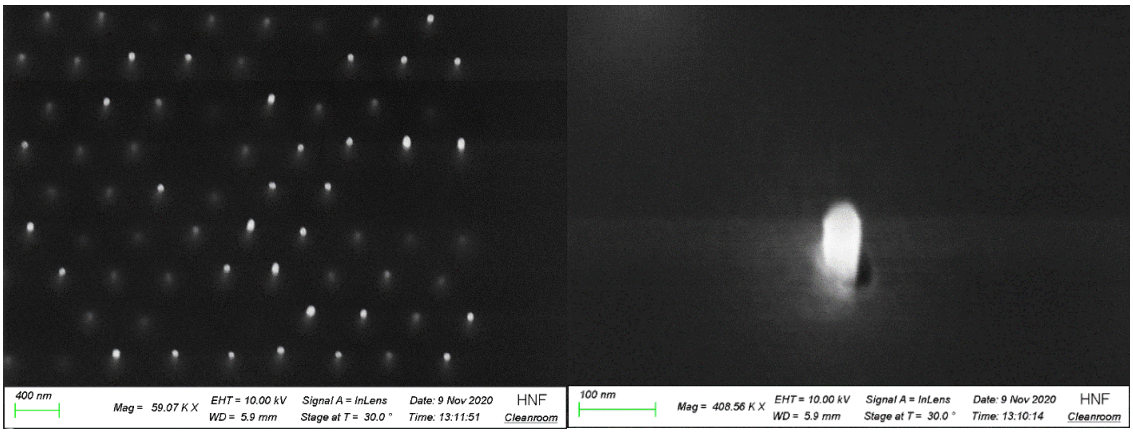


Figure 4-5. The etching rate of HSQ in RIE process.

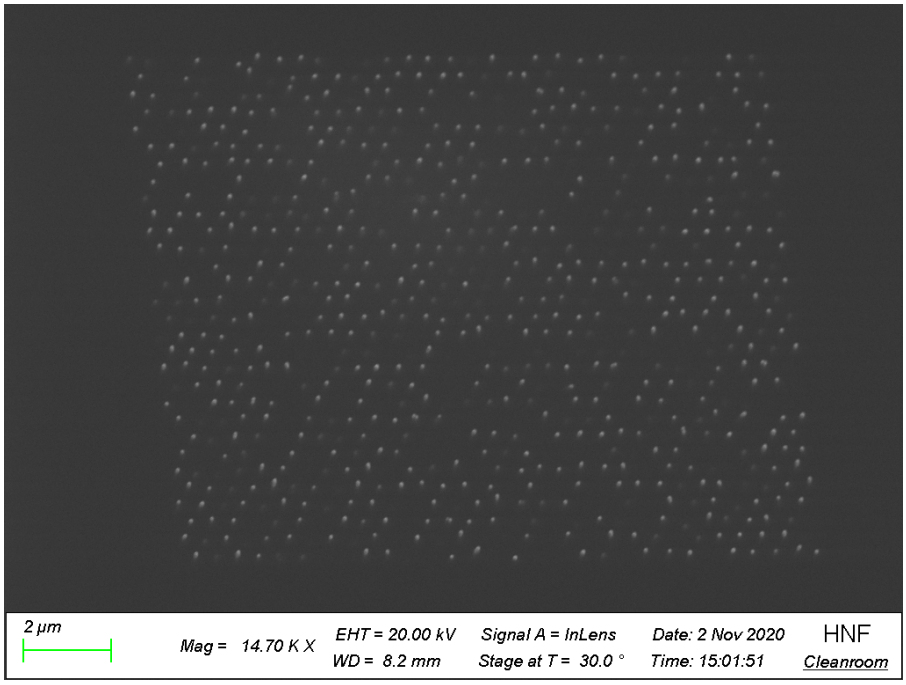


(a)

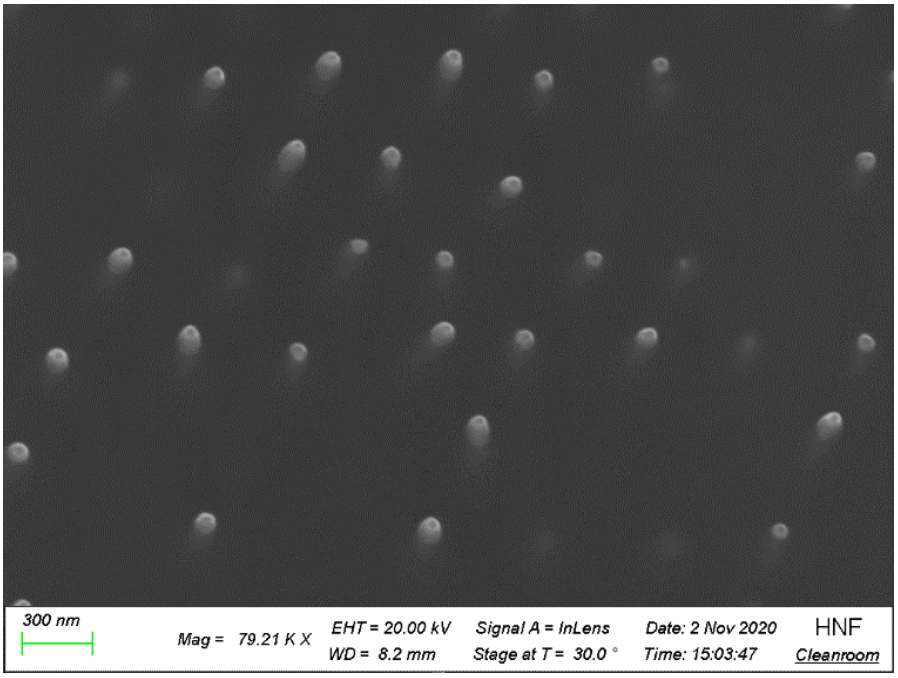


(b) (c)

Figure 4-6. SEM images from the sample with unpassivated InAs nanowires after 5min RIE process (array D40P500). (a) Overview of the nanowire area. (b) and (c) Close-ups of the nanowire area.



(a)

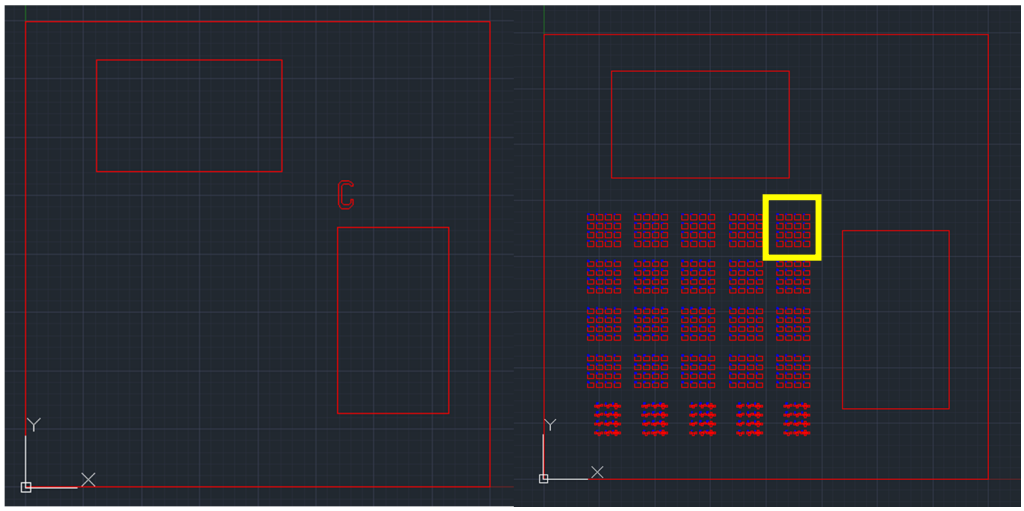


(b)

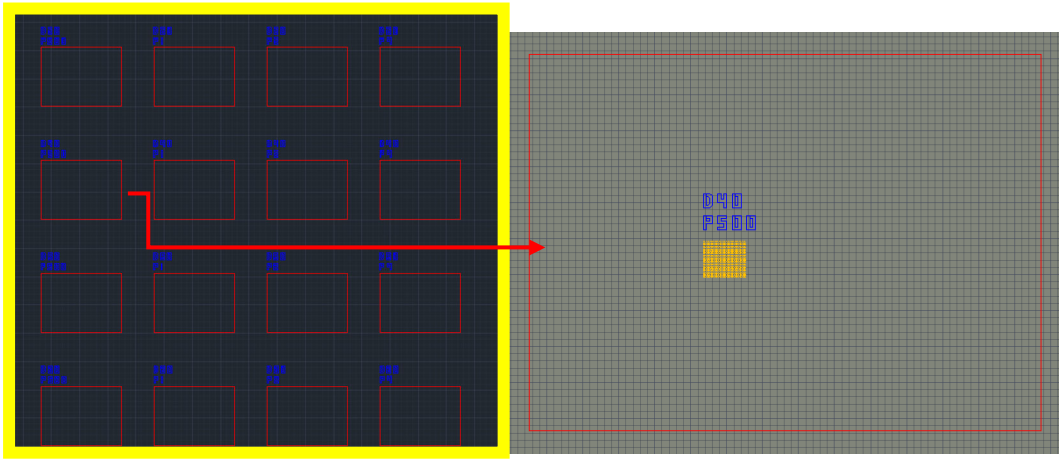
Figure 4-7. SEM images from the sample with Al_2O_3 passivated InAs nanowires after 5min RIE process (array D40P500) (a) Overview of the nanowire area. (b) close-up of the nanowire area.

4.4 Top/bottom electrode fabrication

After exposing the top of nanowires, two photolithography processes are required. The first photolithography is used to open the Si substrate surface for the bottom electrodes. The AutoCAD pattern is shown in Figure 4-8(a). The HSQ in the two rectangles needs to be etched away until the surface of the Si substrate is reached. The second photolithography is to create the resist patterns for metal deposition of the top/bottom electrodes. The AutoCAD design is shown in Figure 4-7 (b) and (c). The metal stack for the top and bottom electrodes is deposited in one process. Close-up of one of the top electrodes is shown in Figure 4-8 (d), the top electrode has a rectangular shape and covers the nanowire array inside. The photoresist AZ5214E is used in both cases, as positive resist for etching and image reversal resist for metal deposition.



(a) (b)



(c) (d)

Figure 4-8. (a) AutoCAD patterns for the first photolithography (sample C). (b) AutoCAD pattern for second photolithography. The upper 4x5 fields are identical and investigated in this thesis. (c) Close-up of the field shown in the yellow square; it contains 4x4 rectangles, each rectangle corresponding to a nanowire array in Figure 2-1 (b) and to a top electrode after the metallization. (c) Close-up of one of the rectangles (array D20P500).

4.4.1 First photolithography

In the first photolithography, the resist AZ5214E was used as positive photoresist, as shown in Figure 4-9 (a)(b) and (c). the detailed process is:

(a) spin-coating of resist AZ5214E with 4000 rpm for 1min and acceleration at 500 rpm/s; then, soft bake at 95°C for 60 s; around 1.4 μm thick resist on the substrate is obtained.

(b) transfer to Maskless Aligner MLA100 and expose with the dose 250 mJ/cm².

(c) development in developer AZ326 MIF for 1min.

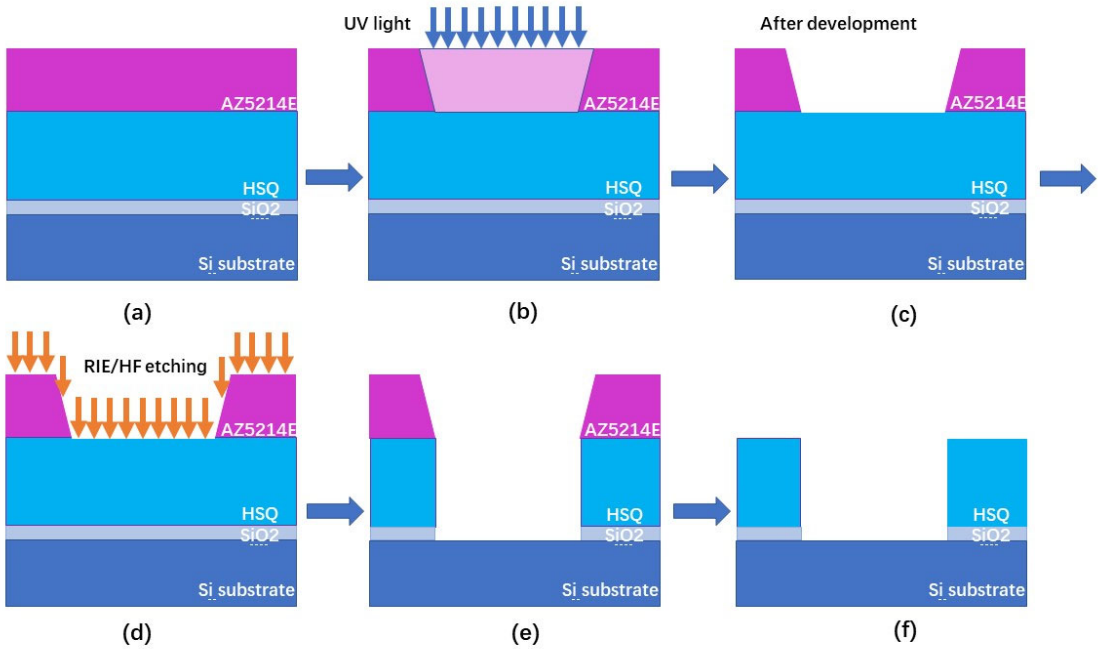


Figure 4-9. Schematic of the first photolithography and RIE processes. This schematic is for sample with unpassivated InAs nanowires For the sample with Al_2O_3 passivated InAs nanowires, there is an Al_2O_3 layer of around 10nm thickness between SiO_2 and HSQ.

During the exposure process, the photoactive compound in the exposed resist area will absorb the incoming ultraviolet light and the light will be attenuated along the path and

the effective exposed area shows a positive slope in depth, as shown in Figure 4-8 (b). As a result, the dissolution rate during development is higher at the top and lower at bottom resulting in a resist with positive slope, as shown in Figure 4-8 (c).

In this thesis, Maskless Aligner-MLA100 was used for the photolithography process. Making a real photomask necessary for the classical mask aligner is time consuming and the pattern cannot be changed once the mask has been fabricated. In comparison, the equipment MLA100 doesn't need a real photomask: the system takes the design file and writes the pattern on the resist-covered substrate with the help of a spatial light modulator. The design file can be redesigned conveniently and the writing time is within minutes, e. g. for the 12.5x12.5mm^2 substrate in this study, the writing process was finished within 5 min. The minimum feature size is 1μm, which is smaller than the minimum structure size of the AutoCAD patterns in Figure 4-7 (a) and (b). The power of the LED light source is 10W at 365nm.

After development, as shown in Figure 4-9 (d) for the sample with unpassivated InAs nanowires, the HSQ and the SiO_2 layer (around 14 nm) are totally etched using a RIE process with CHF_3. For sample with Al_2O_3 passivated nanowires, additionally, there is a Al_2O_3 layer of around 10nm thickness between SiO_2 and HSQ. First, the RIE was used to etch around 500nm thick HSQ and then the rest of HSQ, the Al_2O_3 and SiO_2 layers were etched by HF solution. The real etching time was set slightly higher than the calculated etching time to ensure the reach of the Si surface. This can be checked by ellipsometer. The ellipsometer should show a thickness of SiO_2 under 0.5nm and the value doesn't change when further etching is conducted, which indicates that the Si surface is reached (0 nm SiO_2 cannot be obtained because the Si surface can get very thin oxidation layer in the air and the ellipsometer reaches its limit at this small thickness).

After the etching process, the resist AZ5214E has to be removed. This can be done by putting the substrate in acetone for 30min and in isopropanol for 3min. The immersion time in acetone was longer than normal because the AZ5214E sticks to the substrate tightly after long time RIE process.

4.4.2 Second photolithography

The second photolithography is needed to define the patterns for the top/bottom electrodes. Positive photoresist is suitable for etching processes, but the positive side-walls after development make the lift-off process difficult. Therefore, the image reversal

mode of AZ5214E is needed. The detailed process is illustrated in Figure 4-10 and consists in:

a) spin-coating of resist AZ5214E with 4000rpm for 1min and acceleration 500rpm/s; then, soft bake at 95°C for 60s; around 1.4µm thick resist on the substrate is obtained.

b) transfer to Maskless Aligner MLA100 and expose with the dose 80 mJ/cm².

c) reversal bake of the substrate at 120°C for 120s.

d) flood exposure at Masker Aligner 4 with exposure dose 300mJ/cm^2.

e) development in developer AZ326 MIF for 55s.

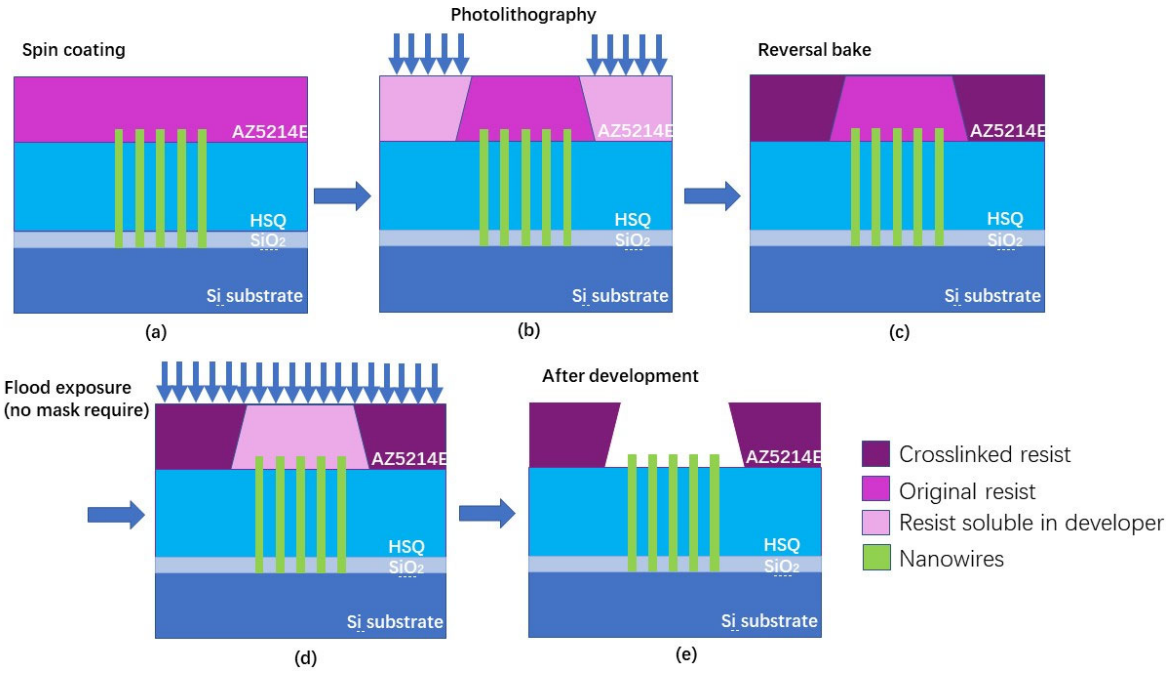
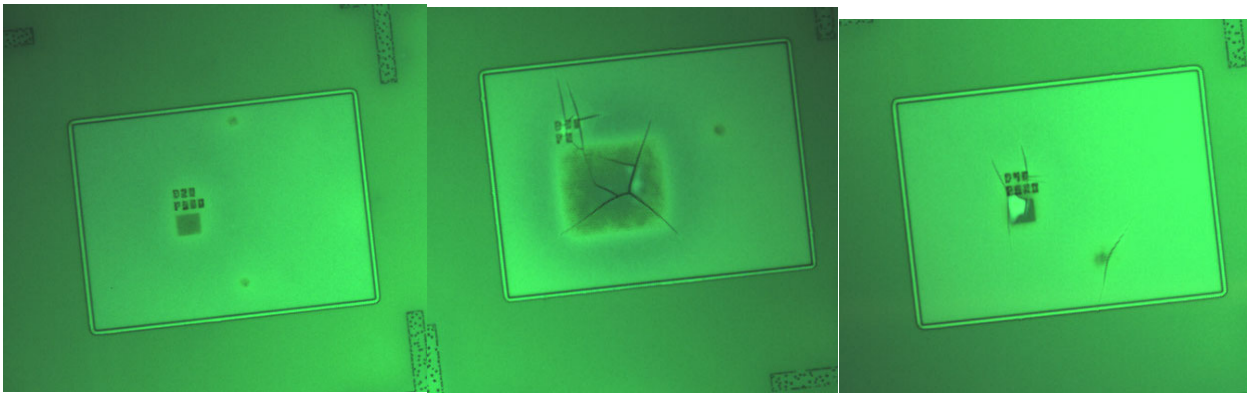


Figure 4-10. Schematic of the process for the second photolithography. Note that the number of nanowires is in reality more than 5. This schematic is for sample with unpassivated InAs nanowires. For the sample with Al_2O_3 passivated InAs nanowires, there is an Al_2O_3 layer of around 10nm thickness between SiO_2 and HSQ.

In the image reversal mode the AZ5214E resist behaves like a negative resist. The role of the reversal bake is to cross link the resist area exposed in the first exposure step, which becomes not light sensitive and almost insoluble in the developer. Through the flood exposure step, the resist in the unexposed area in the previous exposure stepget soluble in developer and is dissolved. After development, the undercut profile of resist which is suitable for lift-off process is obtained.

The results after the development are shown in Figure 4-11 and Figure 4-12. Figure 4-11 shows the patterns of the sample with unpassivated InAs nanowires. The double line of the rectangles indicates the undercut profile of the resist. The right parts of the rectangles beside the nanowire arrays are large enough for the probe contacts used in the electrical measurements. Figure 4-11 (a) shows exemplarily the desired development result. However, many of the patterns have cracks in HSQ layer in the area of the nanowire arrays, as shown in Figure 4-11 (b). In the worst case, the HSQ layer can be peeled off partly also in the region of nanowire array, as shown in Figure 4-11 (c). The reason for the crack formation is not clear, it might be related to the the bad quality of HSQ layer. For the sample with Al_2O_3 passivated InAs nanowires, cracks of the HSQ in the area of nanowire arrays are also present. It is worse in the regions P2 (pitch 2μm) and P4 (pitch 4μm) than for smaller pitches, as shown in Figure 4-12.



(a) (b) (c)

Figure 4-11. Optical microscope images of the sample with unpassivated InAs nanowires after development. (a) pattern with good HSQ layer. (b) pattern with cracks on HSQ layer in the area of nanowire array. (c) pattern with partly peeled-off HSQ layer also the area of nanowire array.

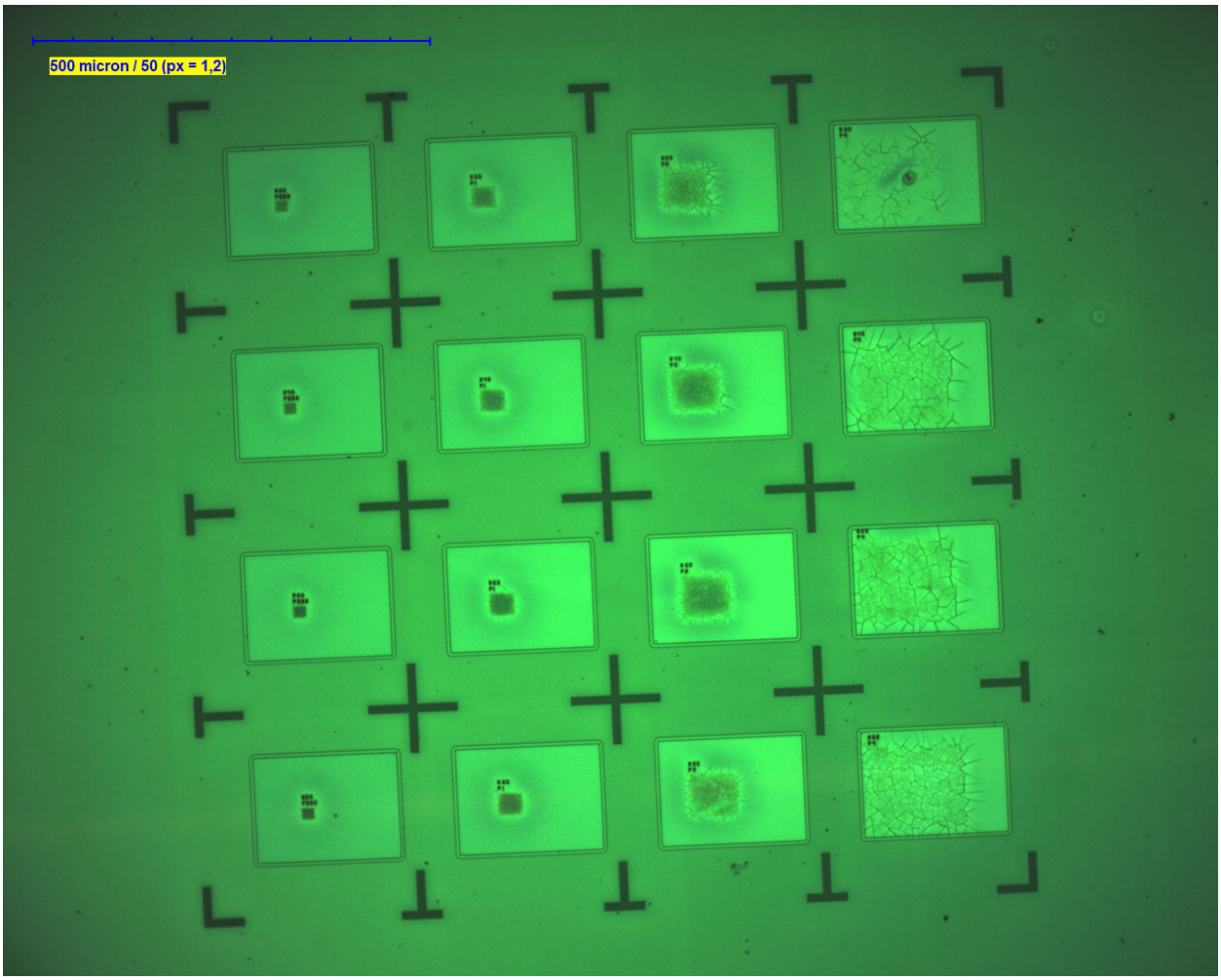


Figure 4-12. Optical microscope images of the sample with Al_2O_3 passivated InAs nanowires after development.

4.4.3 Metallization

Before the metallization process, the samples need to be immersed in 1% HF solution. There are three reasons for this step: 1) After revealing the top of the nanowires by RIE process, the top of nanowires can have residual HSQ which will prevent a good ohmic contact between metal and nanowire top. HSQ can be etched by HF solution as mentioned above. 2) After the RIE process in the first photolithography, the area for the bottom contact is bare silicon surface which can easily oxidize in air and the native oxide layer has to be removed. 3) For the sample with Al_2O_3 passivated InAs nanowires, the Al_2O_3 at the nanowire top needs to be etched in order to create an ohmic contact between InAs and metal. HF solution can be used to etch Al_2O_3 shell selectively.

The etching rate of 1%HF solution on HSQ layer is 10-17 nm/s. For the sample with InAs nanowires, immersion in 1%HF solution for 10s was carried out. The etching rate of Al_2O_3 (ALD grown under 250°C) in 1%HF solution is shown in Table 4-1. For 10nm thick Al_2O_3 shell, 10-15s immersion should be enough. However, for the sample with Al_2O_3 passivated InAs nanowires, immersion in 1%HF solution for 20s was carried out. Not enough HF etching time will result in residual oxide layer on nanowire top and lead to non-ohmic contact.

Table 4-1. Etching rate of ALD deposited Al_2O_3 in 1%HF solution.

Time (s)	etching thickness (nm)	etching rate (nm/s)
5	6.23	1.25
10	9.84	0.98
15	13.51	0.90

After the wet chemical etching, the schematic of the device structure is shown in Figure 4-13(a). The HSQ inside the pattern is thinner than that underneath the resist because of the HF etching. The exact thickness of HSQ in the pattern is studied in Section 5.3. Then, the samples were transferred to the evaporator Univex 400 immediately for the metal deposition. First, 20s in-situ Ar sputtering was carried out to remove possible native oxidation and then 20nm thick Ti layer and 300nm thick Au layer were deposited sequentially (Figure 4-13(b)). Afterwards the samples were immersed in acetone for 1h for the lift-off process (Figure 4-13(c)), which means that the excess metal was lifted off with the removal of the resist. Finally, the samples were immersed in isopropanol for 3min and dried with nitrogen gun. In this way, the top and bottom metallic pads were fabricated successfully (Figure 4-13(d)) and the samples were ready for electrical measurements.

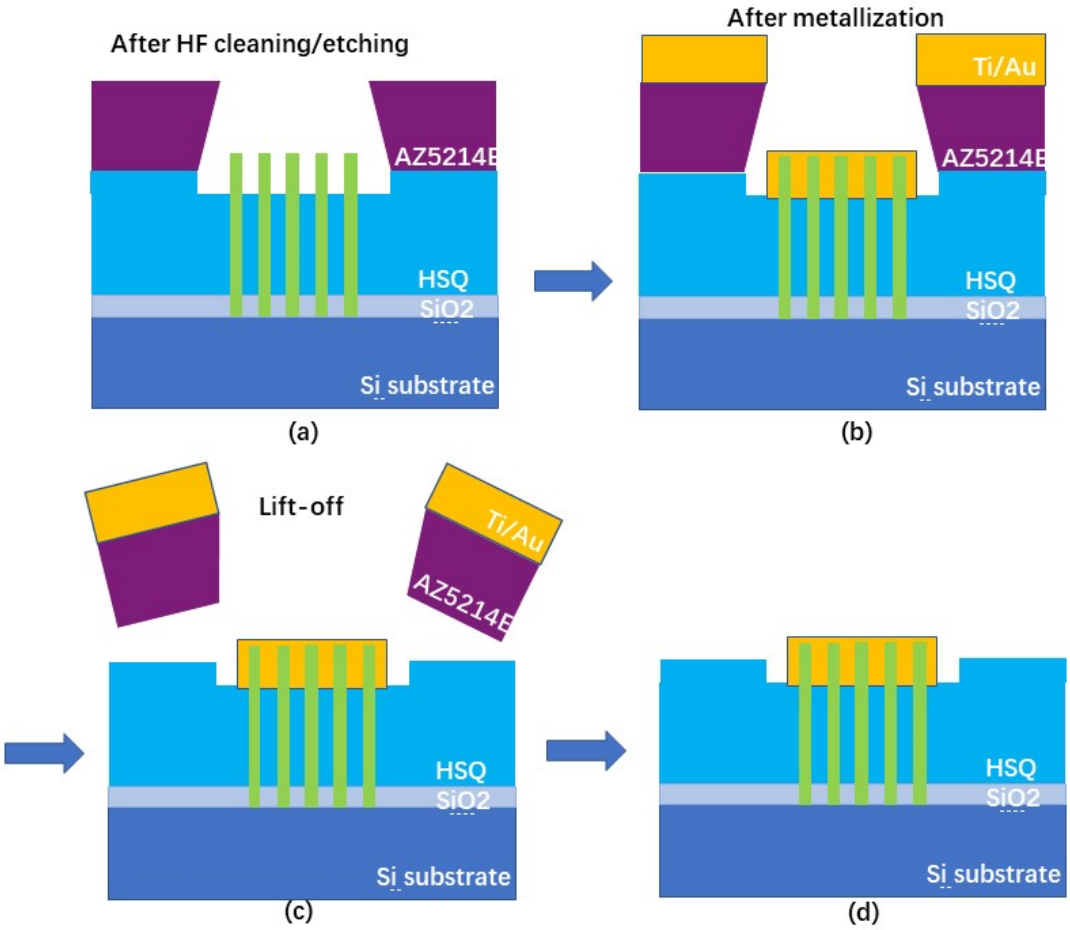


Figure 4-13. Schematic of the metallization process. After the metallization process, Ti/Au contacts on the the nanowire arrays have been obtained.

The bottom electrode only needs to guarantee ohmic contact and low resistance, while the top electrode fabrication is more crucial. Exemplarily, SEM images for the sample with unpassivated InAs nanowires are shown in Figure 4-14. Figure 4-14 (a) shows the top electrode on the label and nanowire array and (b) and (c) are the same metallization areas with higher magnification. The bright points in these images show the top of nanowires, therefore the number of nanowires under the top electrode in the nanowire array as well as in the label can be counted. Exemplarily, the counting method is shown in Figure 4-15 where the yellow circles represent the top of nanowires. As shown in Figure 4-16, the number of nanowires in the nanowire array is 326 (Figure 4-16 (a)) and the number of nanowires in the label is 99 (Figure 4-16 (b)). Therefore, the number of nanowires connected by top electrode is totally 425.

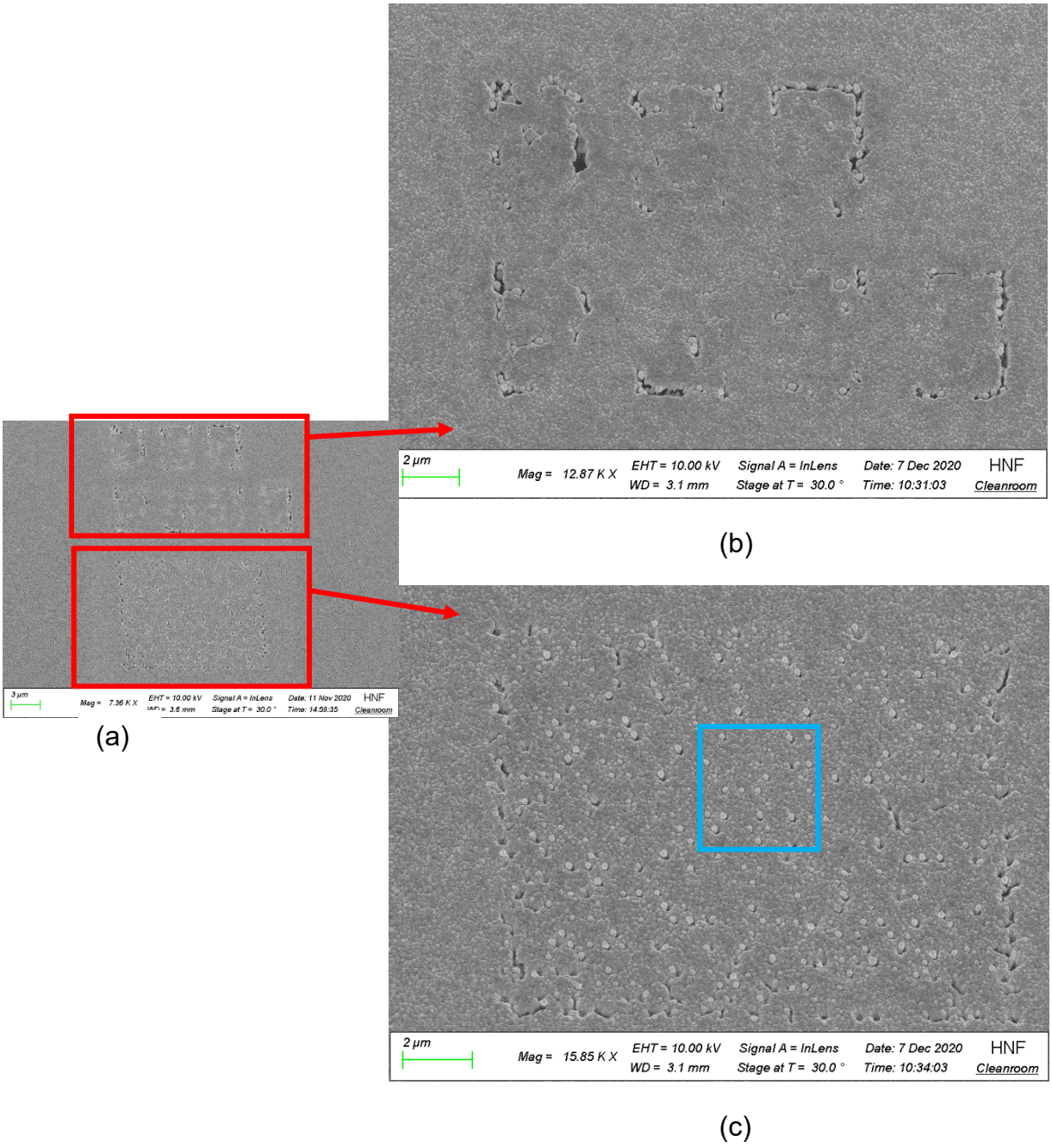
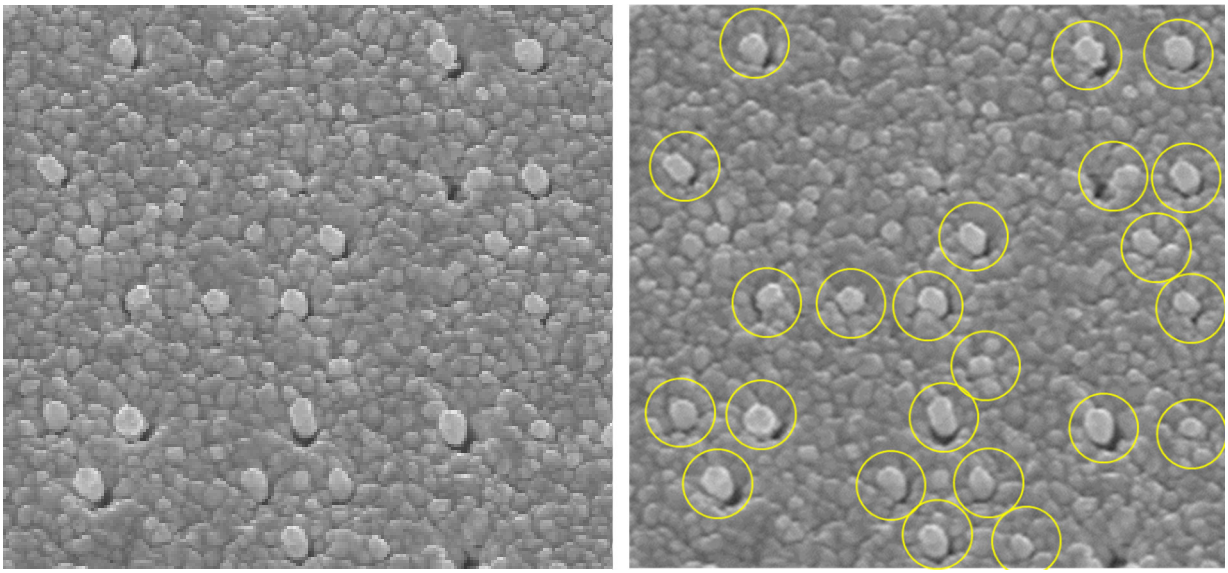
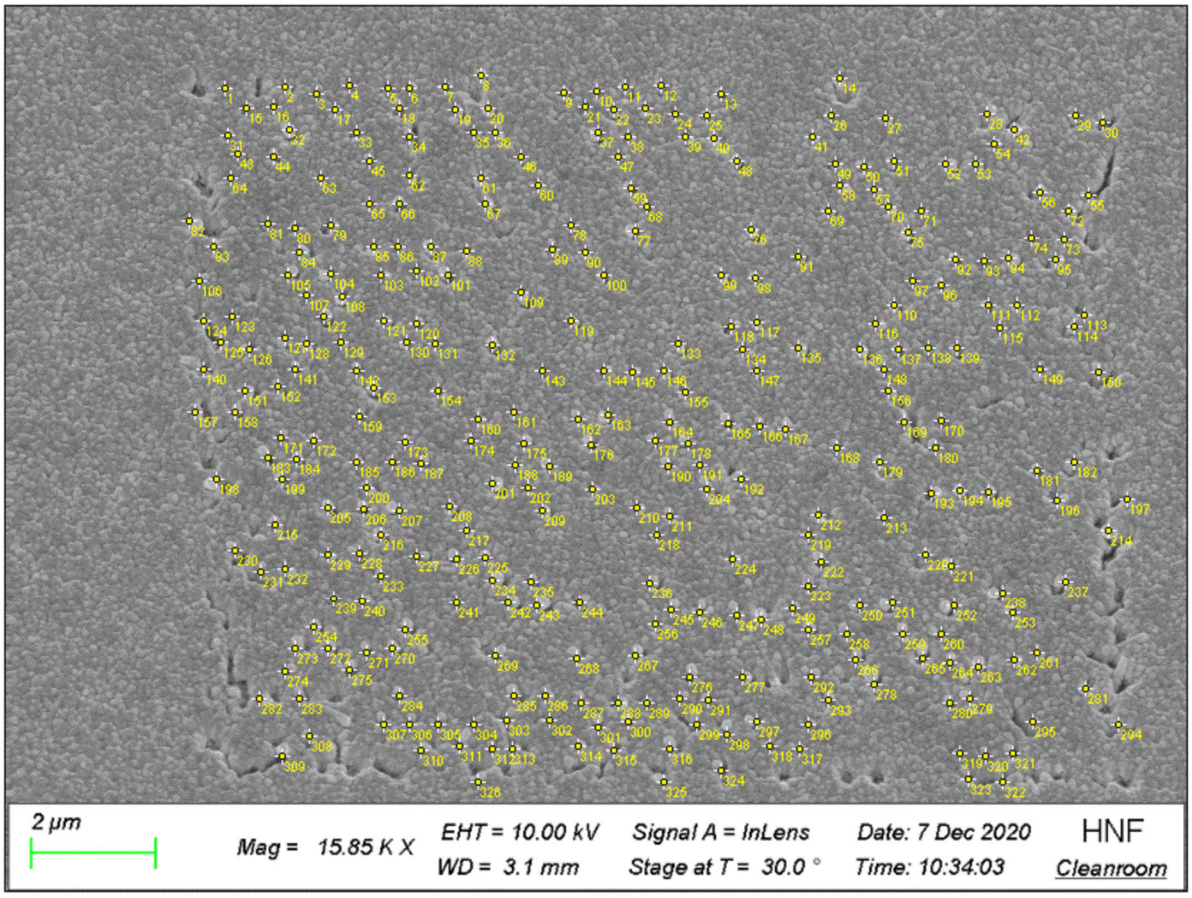


Figure 4-14. SEM images of a top electrode (region D20P500) for sample with unpassivated InAs nanowires. The two red rectangles in (a) represent the label (b) and the nanowire array (c) respectively.

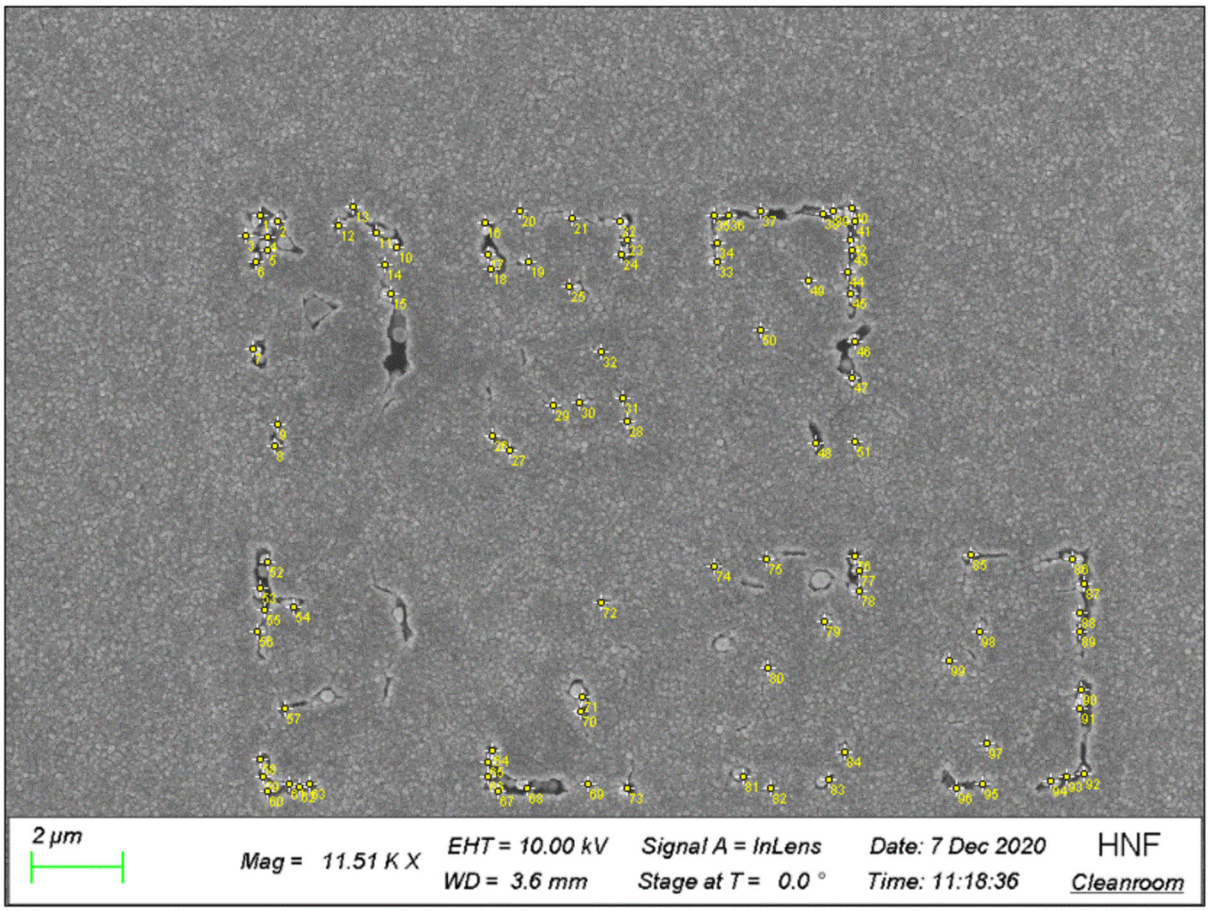


(a) (b)

Figure 4-15. (a) SEM image of the blue rectangular area in Figure 4-14 (c). (b) the connected nanowires are marked with yellow circles.



(a)



(b)

Figure 4-16. (a) Counting of the nanowire number in the nanowire array of Figure 4-14. (b) Counting of the nanowire number in the label of Figure 4-14.

The SEM images for the sample with Al_2O_3 passivated InAs nanowires are shown in Figure 4-17. The quality of the metallization is worse than for the sample with unpassivated InAs nanowires. There are many cracks in the metal layer because 1%HF etching was longer with 10s in comparison with the time used for the sample without passivation, as discussed in section 4.4.3. The etching rate of HSQ in 1%HF is 10-17nm/s. Thus, the side effect is that the cracks in HSQ layer are enlarged, and the thickness of HSQ layer is around 100-170nm thinner than in the sample with unpassivated InAs nanowires. The number of connected nanowires by top electrode can also be calculated, but the number is not easy to determine because the top of some of nanowires is too long to be connected by the electrode. Exemplarily, the close-up of the blue rectangular area in Figure 4-17 (c) is shown in Figure 4-18. The yellow circles represent the nanowires which are well connected with top electrode, the red circles represent the nanowires which are not sure whether they are connected or not, and the blue circles represent the

nanowires which are certainly not connected. The number of nanowires in the label is also counted in the same way. For the nanowire array-based device in Figure 4-17 (a), as shown in Figure 4-19, the connected nanowire number is between 386 (only yellow number included)-527 (red number and yellow number included).

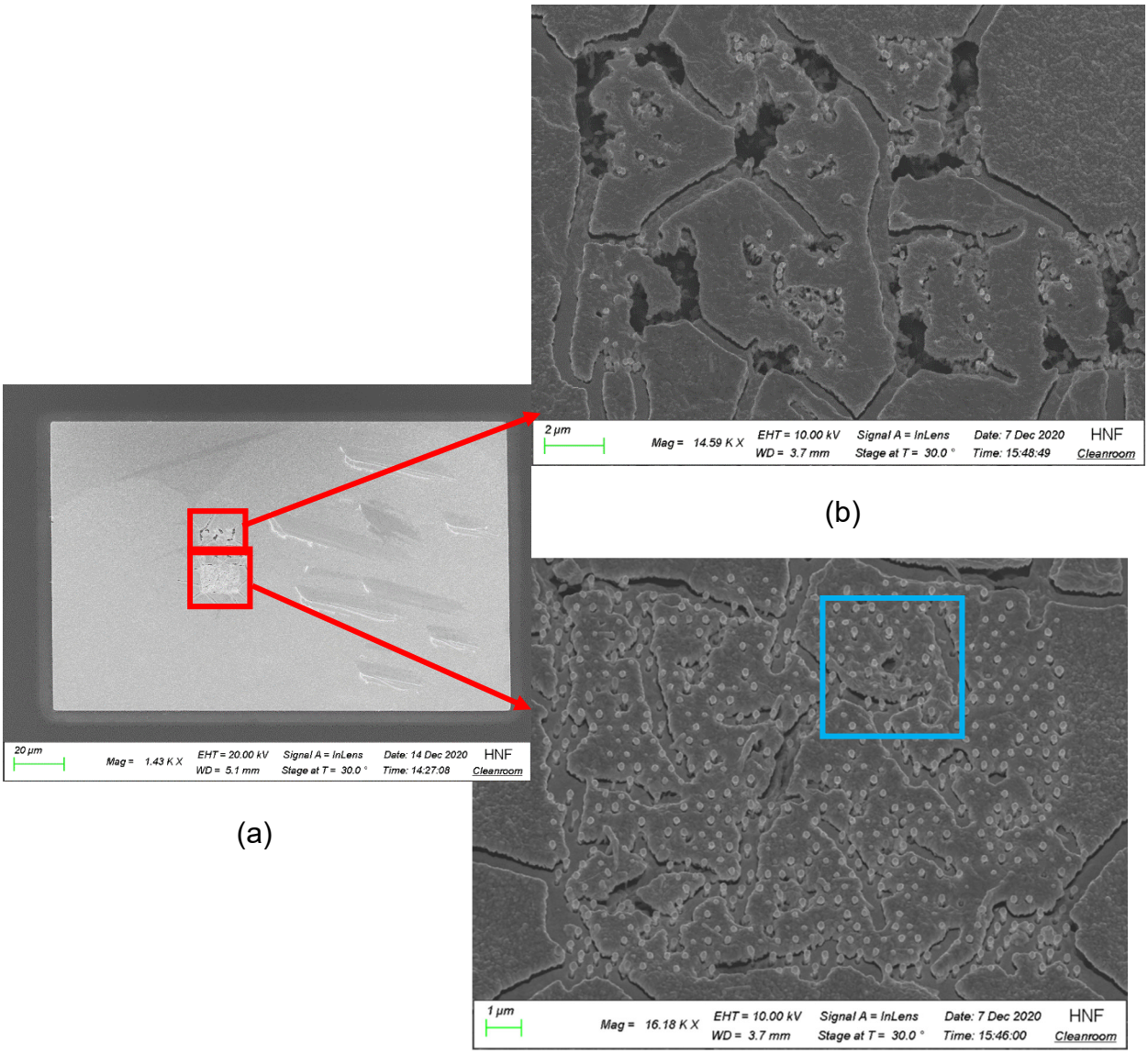
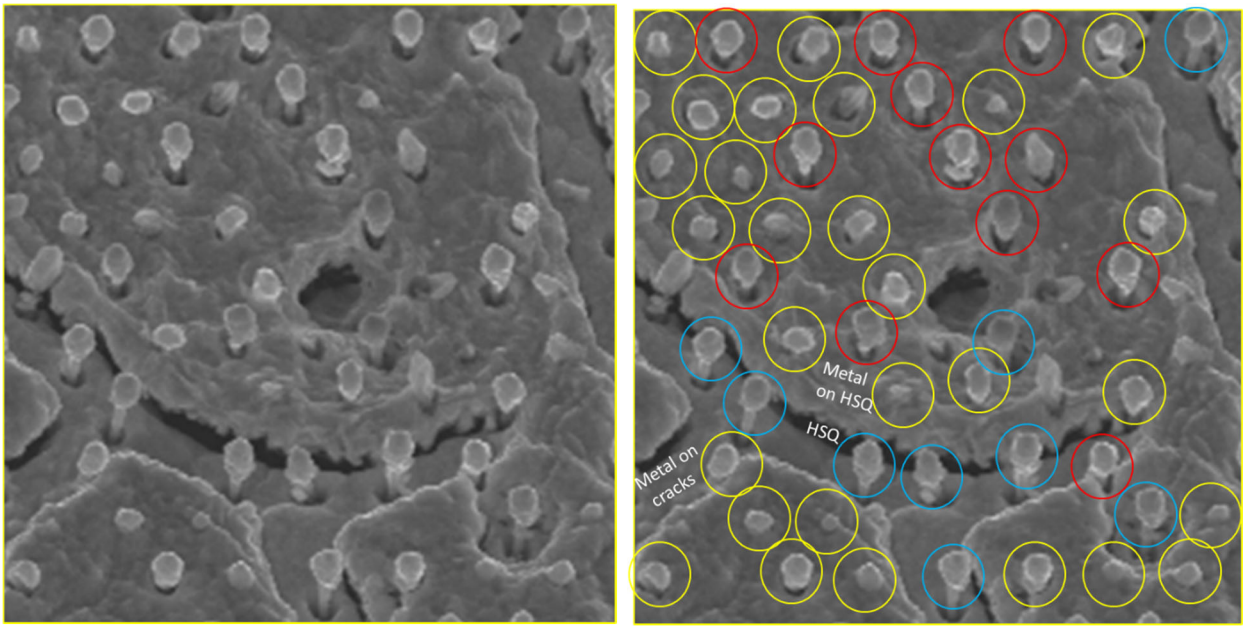
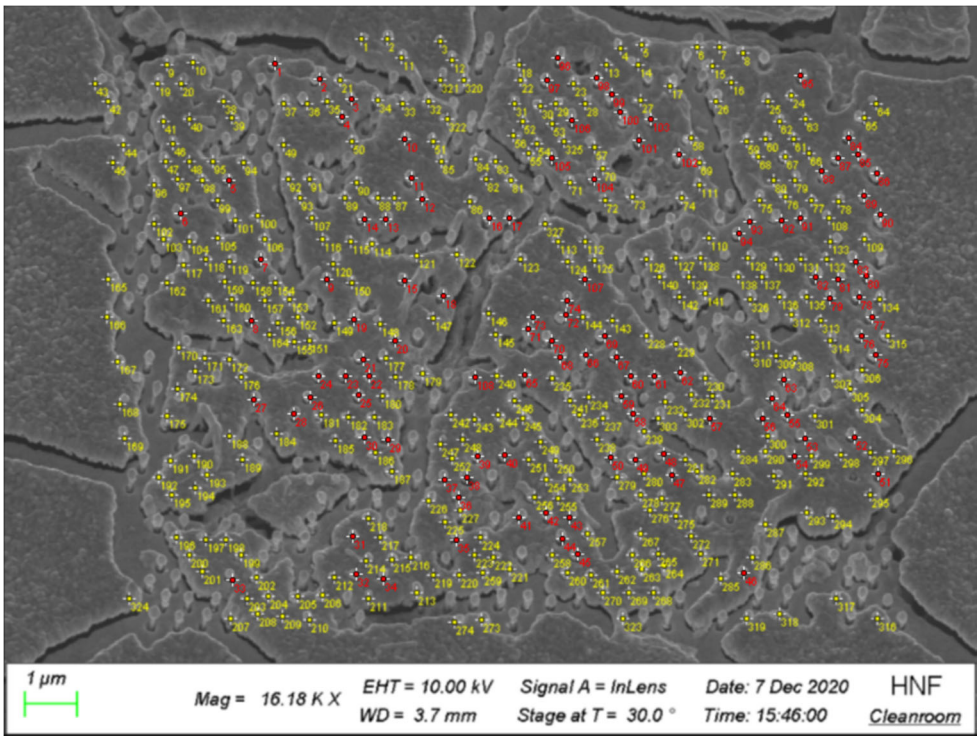


Figure 4-17. SEM images of a top electrode (region D20P500) for sample with Al_2O_3 passivated InAs nanowires. (a) The overview of the top electrode. The two red rectangles represent the label (b) and the nanowire array (c). The scratches on the right side are traces after the use of the probesfor the electrical measurements.

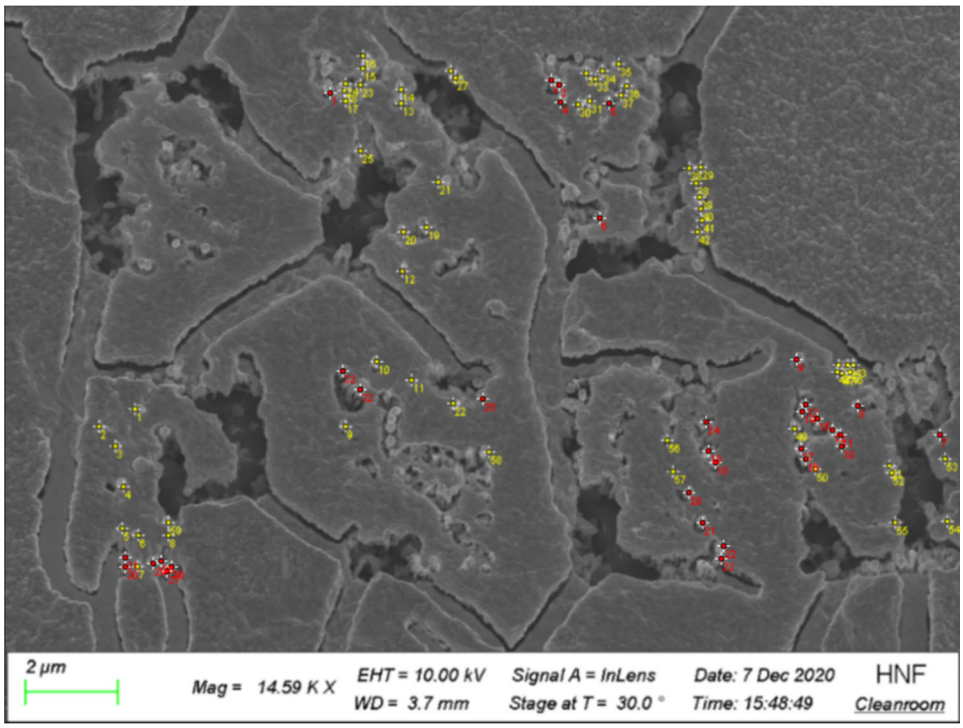


(a) (b)

Figure 4-18. (a) SEM image of the blue rectangular area in Figure 4-17 (c). (b) the counting method of connected nanowires. The nanowires in the cracks are not connected by the top electrode; the metal deposited on cracks is isolated from bottom electrode because there is still 14nm SiO_2 layer plus around 10nm thick Al_2O_3 layer on the Si substrate.



(a)

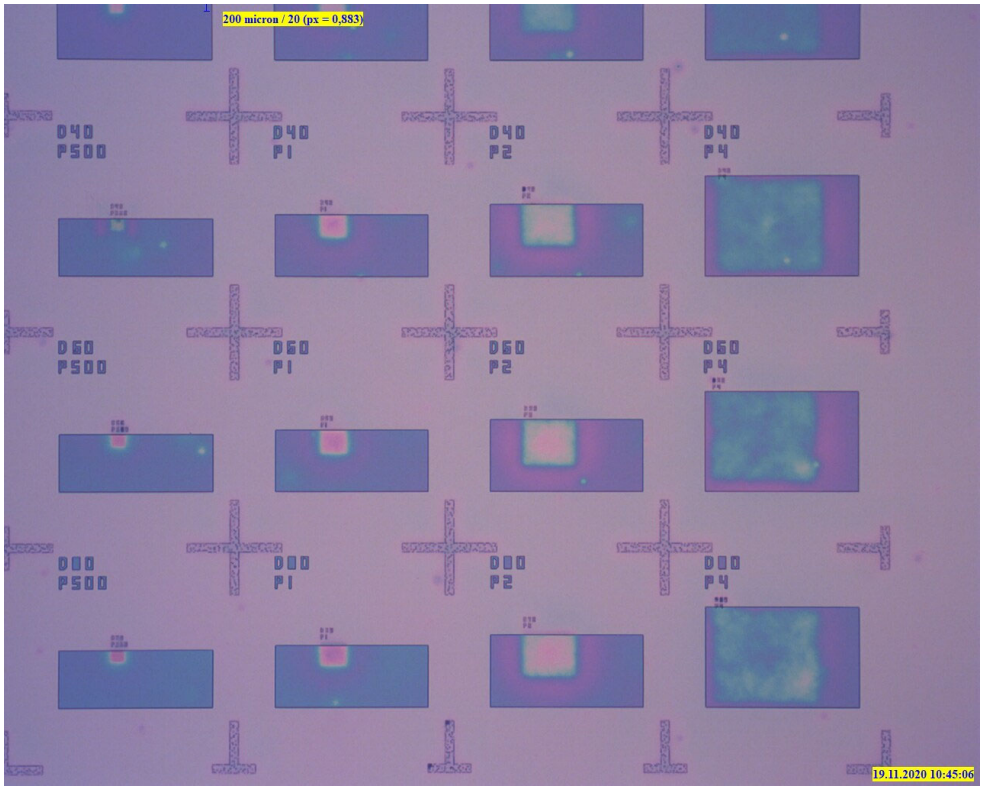


(b)

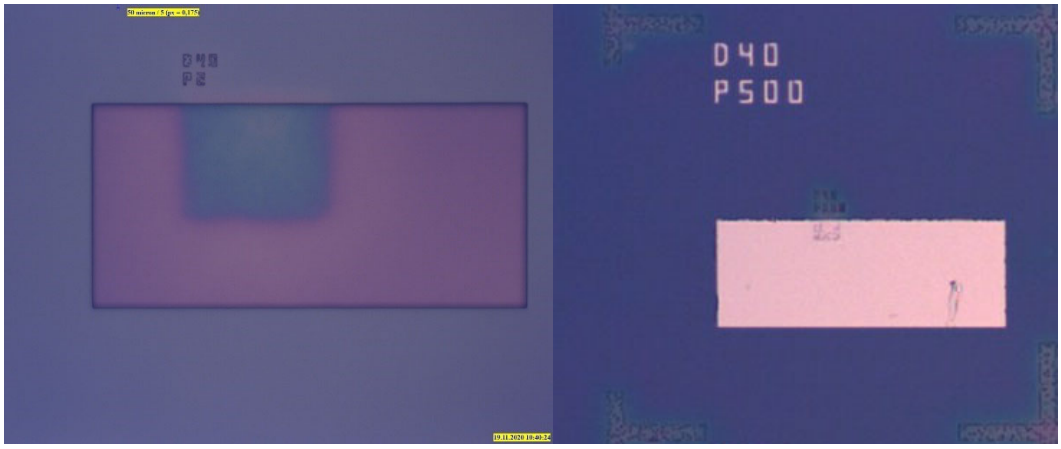
Figure 4-19. (a) Counting of the nanowire number in the nanowire array of Figure 4-17. (327 in yellow, 108 in red). (b) Counting of the nanowire number in the label of Figure 4-17. (59 in yellow, 33 in red). Red numbers mean uncertain connected nanowires, yellow numbers mean certain connected nanowires. Totally the nanowire number is 386 in yellow and 527 in yellow plus in red.

4.5 Attempt to improve the quality of HSQ

The troublesome point is that many of the top electrodes have cracks in the nanowire array area due to HSQ cracking. To improve the quality of HSQ layer, 5 min oxygen plasma 200W/80sccm and then RTP with curing temperature 400°C for1h was performed on a sample with unpassivated InAs nanowires. The improvement of HSQ layer was significant, after development there are no cracks in HSQ layer as shown in Figure 4-18 (a) and (b). this indicates that oxygen plasma and higher curing temperature increase the resistance of HSQ against development. Afterwards, 45s 1%HF etching was used before metallization (longer time is due to much lower etching rate). After metallization, the top electrodes also show smooth surface and without cracks, as shown in Figure 4-18 (c).



(a)

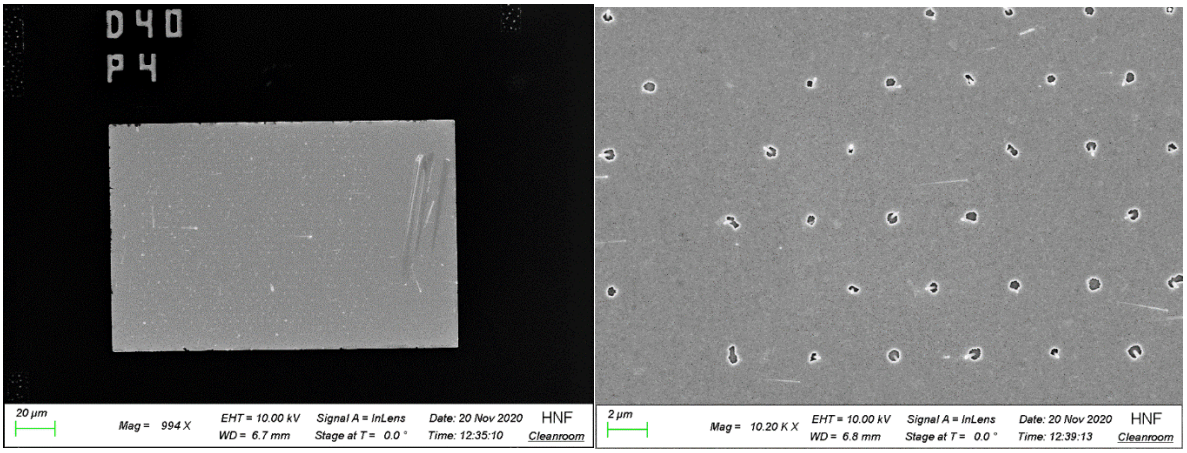


(b) (c)

Figure 4-18. (a) and(b) Optical microscope images of a sample with unpassivated InAs nanowires after oxygen plasma treatment and RTP at 400°C for 1h . (c) The result after metallization.

As presented in [45], the thickness and porosity of HSQ will decrease with increasing curing temperature, and the HF etching rate will decrease with decreasing porosity. In my study, the thickness of one single HSQ layer is 200nm at curing temperature 300°C/15min

and is 177nm at curing temperature 400°C for 1h. The HF etching rate is 10-17nm/s at curing temperature 300°C for 15min and less than 1.2nm/s at curing temperature 400°C for 1h. Therefore, higher curing temperature 400°C is used to reduce the HF etching rate and it is expected that the HSQ layer thickness is more controllable after HF etching before metallization and also InAs nanowire length inside HSQ is more controllable. But the low HF etching rate is only the property for HSQ layer in the opened area. For the HSQ around nanowires, the HF etching rate is much higher than that in an opened area. A possible explanation is given in [45], the silsesquioxane network around sidewalls is strengthened and can resist the compression under high curing temperature. Therefore, the HSQ area around nanowires still has low density and high porosity and the HF etching rate is higher than in open area. Thus, 45s HF etching results in the formation of a hole around each nanowire and after metallization many of the nanowires are not connected with top electrode, as observed in Figure 4-19 (b). Another problem is that the I-V characteristics measured between -0.5V and 0.5V is not linear and the resistance is very high. The reason could be the decomposition of InAs when annealing at 400°C for 1 hour, which could influence the surface property of InAs and affect the contact resistance between InAs and Ti/Au metallization. Similar results are also obtained for a sample with Al_2O_3 passivation.



(a) (b)

Figure 4-19. SEM images of the sample with unpassivated InAs nanowires after metallization. (a) Overview of the top electrode with HF etching time before metallization 45s. (b) Close-up of the top electrode shown in (a).

Due to the exposed problems, this method was not adopted. In the next section, the electrical measurements are based on the initial preparation method of the HSQ planarization layer.

5. Electrical measurements and results

5.1 Calculation of nanowire resistivity

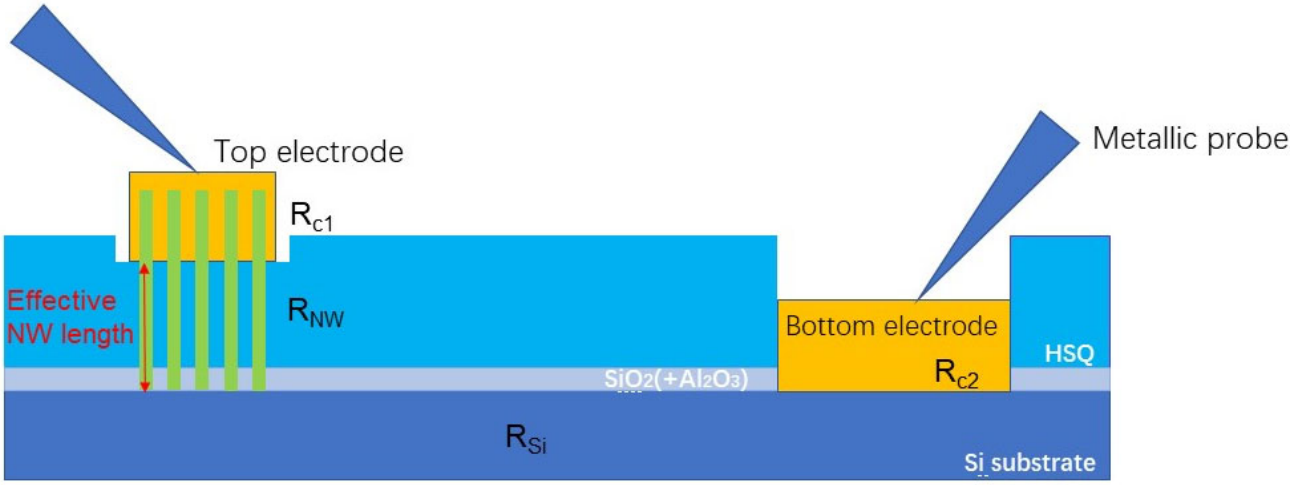


Figure 5-1. Schematic of resistance along the circuit. The effective nanowire length is the nanowire length between top electrode and bottom substrate.

As shown in Figure 5-1, the resistance along the circuit consists of the contact resistance R_{C1} between Ti/Au top electrode and InAs nanowires, the resistance along InAs nanowire array R_{NW}, resistance along Si substrate R_{Si}, and contact resistance R_{C2} between Ti/Au and Si substrate.

$$R=V/I= R_{C1}+ R_{NW} + R_{Si} + R_{C2} \quad (5.1)$$

For the device configuration in this study, the contact resistance R_{c1} cannot be determined. The Si substrate is n-doped with a resistivity < 0.005 Ω*cm. Therefore, the R_{Si} can be neglected. As mentioned in section 1.5.2, the Ti/Au-Si bottom contact is ohmic because the silicon substrate is heavily n-doped R_{C2} is also neglected in this thesis. Therefore, the inverse slope of the I-V curve can be considered as the sum of the top contact resistance and the resistance along the nanowire array, namely:

$$R=V/I= R_{C1}+ R_{NW} \quad (5.2)$$

The ‘n’ nanowires in one array are connected in parallel, thus

$$R=V/I=R_{C1}+ R_{NW}= (R_{SC1}+ R_{SNW})/n \quad (5.3)$$

in which R_{SC1} means the top contact resistance of single nanowire and R_{SNW} means the resistance along single nanowire.

In this study, the cross-section A and physical composition of nanowires can be considered as uniform along the length, the resistivity ρ of a nanowire can be calculated as:

$$\rho = R_{SNW} * A/L \tag{5.4}$$

here A is the cross section of a nanowire, L is the effective nanowire length.

The InAs grown nanowires have hexagonal cross section:

$$A = \frac{3\sqrt{3}}{8} d^2 \tag{5.5}$$

here d is twice of the hexagon side length, which can be considered as the diameter of nanowires.

Therefore, the resistivity ρ of a nanowire is:

$$\rho = R_{SNW} * \frac{3\sqrt{3}d^2}{8L} \tag{5.6}$$

5.2 I-V characteristics of the InAs nanowire-array based devices

The I-V characteristics of the processed devices was measured with a Keithley 4200A probe station. This probe station has 4 metallic probes, which can be used to perform two or four terminal measurements. In this study, to contact the top and bottom electrodes, only two probes are needed, as shown in Figure 5-1. The voltage was applied on top electrode and the bottom electrode was connected to the ground. The applied voltage varies between -0.5V to +0.5V and the corresponding current can be measured.

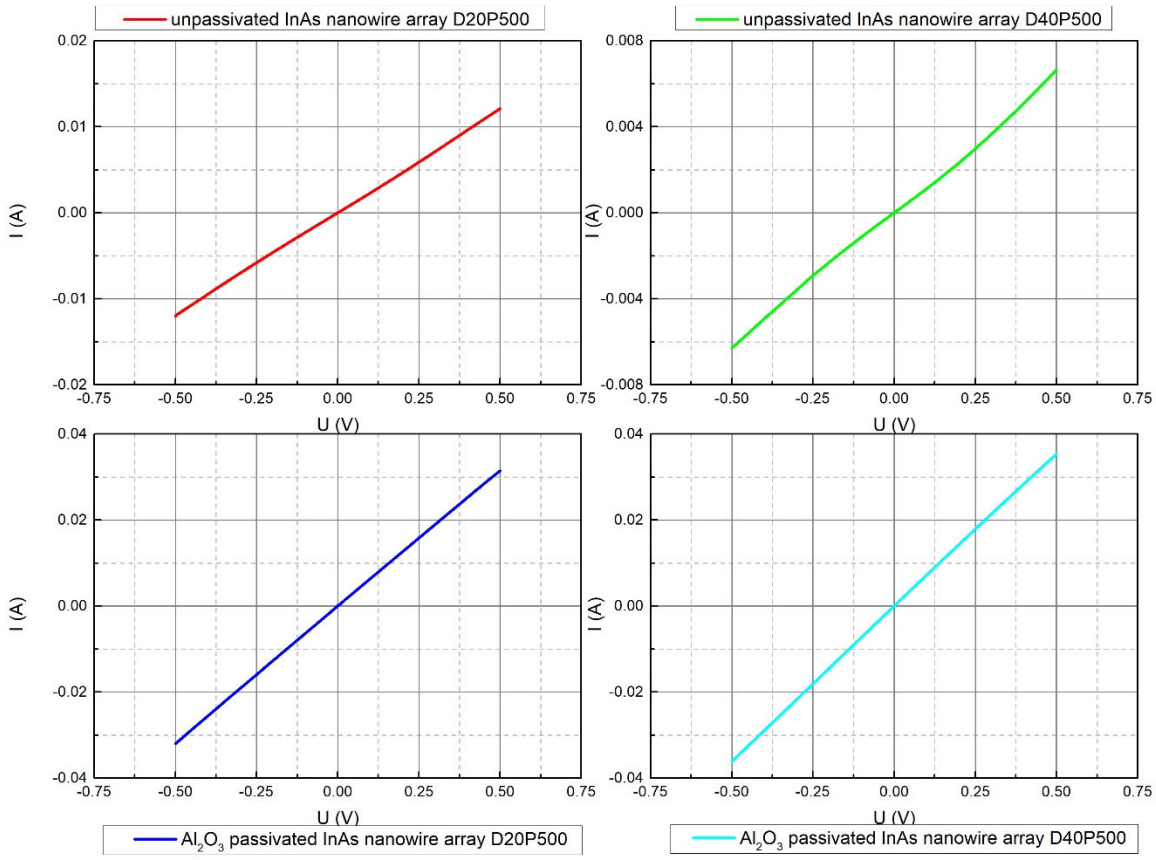


Figure 5-2 I-V characteristics of different InAs nanowire-array based devices.

The I-V characteristics are Ohmic and reflects the resistance of the nanowire array. The nanowire number has to be taken into account to obtain the resistance of single nanowire as show in formula (5.3). Table 5-1 shows the nanowire number and resistance information. The normalized I-V characteristics are shown in Figure 5-3. It is obvious that the resistance of the nanowires with Al_2O_3 passivation is lower than that of the nanowires without passivation.

Table 5-1 Nanowire array resistance and single nanowire resistance

	Resistance of nanowire array	Nanowire number	R_{SC1}+ R_{SNW}
Unpassivated InAs nanowire array D20P500	41.49Ω	421	17.47kΩ
Unpassivated InAs nanowire array D40P500	75.3Ω	186	14.01kΩ
Al_2O_3 passivated InAs nanowire array D20P500	15.9Ω	386-527	6.14-8.38kΩ
Al_2O_3 passivated InAs-nanowire array D40P500	14.17Ω	414-446	5.87-6.32kΩ

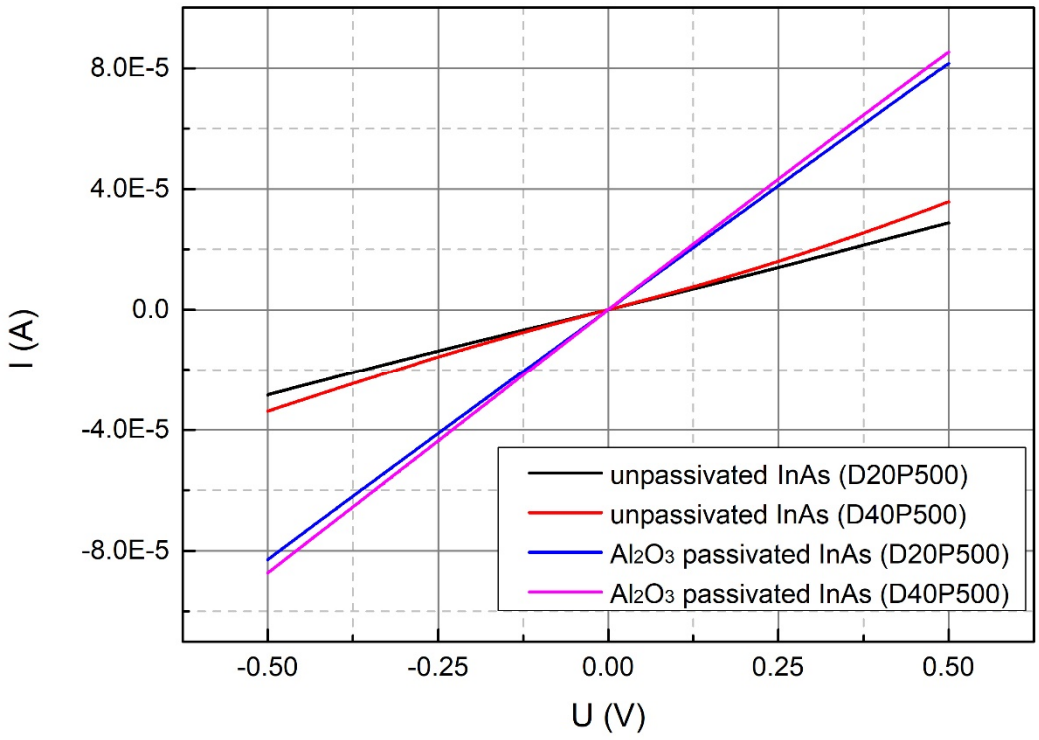
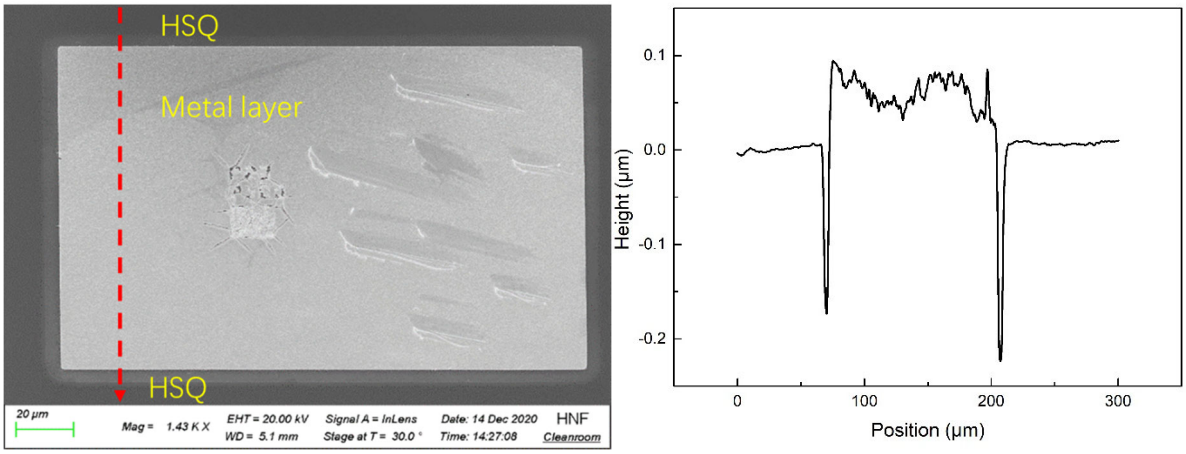


Figure 5-3. I-V characteristics of single nanowires obtained by normalization of the measured current to the number of nanowires in the arrays. For Al_2O_3 passivated nanowires, the curves are based on the lowest nanowire number (386 and 414).

5.3 Determination of the effective nanowire length

To calculate the resistivity of single nanowire according to equation (5.6), the effective nanowire length L_{nw} need to be determined which can be achieved by Dektak XT. Dektak XT is a stylus profilometer. During the measurement, the diamond-tip stylus contacts the sample surface, the stylus force is kept constant and the sample moves with the sample stage following the sample profile. Therefore, the surface topography of the measured

path can be recorded. In our measurement, the stylus moves along the red line as shown in Figure 5-4 (a) and the height of the profile can be obtained as shown in Figure 5-4 (b). Through this method, the height difference between the HSQ layer and the metal layer can be calculated.



(a) (b)

Figure 5-4 (a) The moving path of Dektak XT stylus. (b) The height profile from the Dektak measurement.

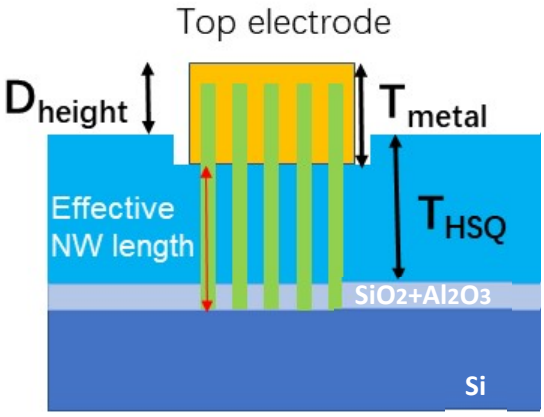


Figure 5-5 The schematic of the thickness relationship of each layers on a device.

For sample with Al_2O_3 passivated InAs nanowire array, D_{height} obtained from the Dektak measurement is in average 35.6nm. Given that the thickness of HSQ layer T_{HSQ} is 529.4nm, the thickness of metal layer(Ti/Au) is 320nm, the thickness of SiO_2 layer T_{SiO2} is 14nm and the thickness of Al_2O_3 layer T_{Al2O3} is 10 nm, and according to Figure 5-5 and

$$L_{NW} = T_{HSQ} - (T_{metal} - D_{height}) + T_{SiO2} + T_{Al2O3} \quad (5.7)$$

the effective length of nanowire is 269 nm.

Similarly, D_{height} for the sample with unpassivated InAs nanowire array can be obtained from Figure 5-6 and it is in average 221.9nm. Given that the thickness of HSQ layer T_{HSQ} is 514.5nm, the thickness of metal layer(Ti/Au) is 320nm, the thickness of SiO2 layer T_{SiO2} is 14nm, and according to

$$L_{NW} = T_{HSQ} - (T_{metal} - D_{height}) + T_{SiO2} \quad (5.8)$$

the effective nanowire length for sample with InAs nanowire array is 430.4nm.

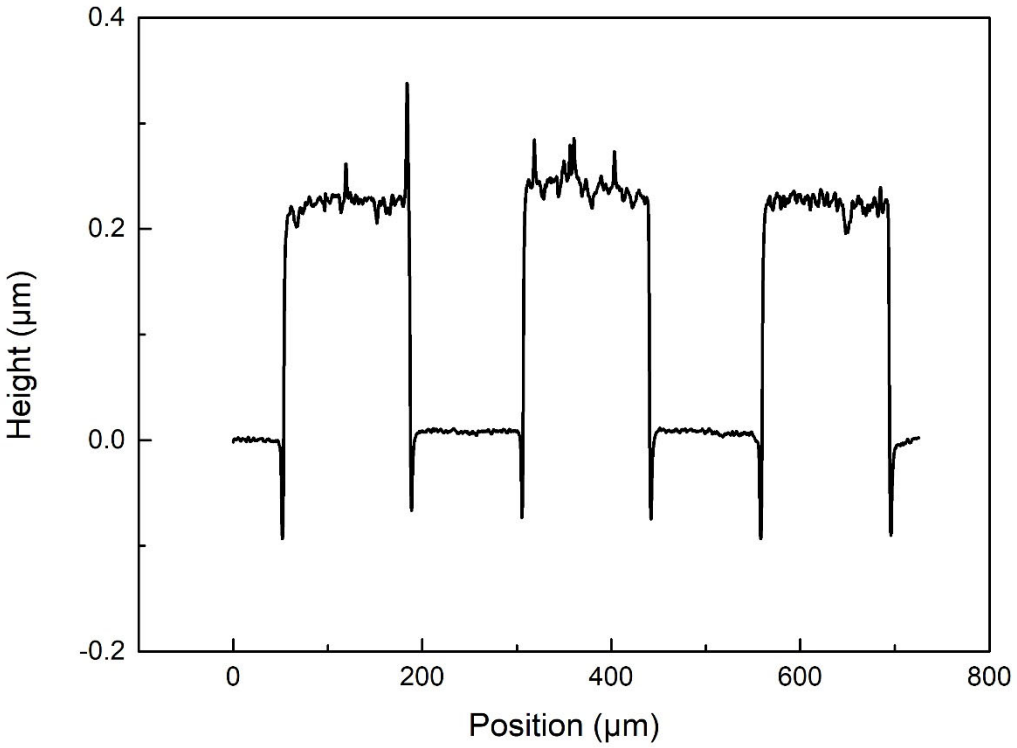


Figure 5-6. The height profile of three top electrodes from Dektak measurement.

5.4 Resistivity results

The nanowire diameter from different nanowire arrays can be obtained from SEM images with the help of the software ImageJ [46]. All the results are shown in Table 5-2. The diameter of Al_2O_3 passivated InAs nanowires in the array D20P500 is in average 65.2nm

and in the array D40P500 is in average 69.3nm. (The standard deviation for all results is within 5nm.) The diameter of InAs core need to be determined. Because the unavailability of STEM and TEM, the diameter cannot be determined directly. But because on the two samples (with and without Al_2O_3 passivation), the InAs nanowires have been grown in the same growth conditions the InAs core diameter for the sample with Al_2O_3 shell is estimated to be the same as the diameter for sample with unpassivated InAs nanowire. The InAs nanowries are all undoped, thus the measured resistance is mainly contributed on nanowires themselves, the contact resistance R_{sc1} can be neglected. Therefore, the resistivity can be obtained according to the equation (5.6). The results are shown in Table 5-2. The resistivity is over estimated due to the neglected resistances R_{C1}, R_{Si} and R_{C2}.

Table 5-2 Nanowire resistivity information

	R_{SNW} /kΩ (R_{sc1} neglected)	InAs Nanowire diameter d/nm	Effective nanowire length L/nm	Resistivity ρ/Ω*cm (over estimated)
Unpassivated InAs nanowire array D20P500	17.47	49.8	430.4	$6.5x10^{-3}$
Unpassivated InAs nanowire array D40P500	14.01	53.5	430.4	$6.0x10^{-3}$
Al_2O_3 passivated InAs nanowire array D20P500	6.14-8.38	49.8	269	$3.7x10^{-3}$ ~ $5.0x10^{-3}$
Al_2O_3 passivated InAs nanowire array D40P500	5.87-6.32	53.5	269	$4.1x10^{-3}$ ~ $4.4x10^{-3}$

The conclusion is that for nanowire array with average diameter 49.8nm, the resistivity of InAs nanowire with Al_2O_3 passivation is 57%-77% of the value without passivation. For nanowire array with average diameter 53.5nm, the resistivity of InAs nanowire with Al_2O_3 passivation is 68%-73% of the value without passivation. The conductivity of InAs nanowires has increased and it can be asserted that by passivation of the InAs nanowire surface by Al_2O_3, the electron mobility in InAs nanowires increases due to the reduced surface scattering.

6. Summary and outlook

A new method for the selective MBE growth of InAs nanowire arrays on prepatterned SiO_2/Si(111) substrates was developed. In this method, H_2O_2 is used to create a thin oxide layer on the Si(111) surface in the patterned SiO_2 holes. The main role is played by the Ga assisted surface modification procedure prior to InAs nanowire growth, in order to create pinholes as nucleation sites for the nanowires. Using this method high reproducibility and high yield of vertical nanowires are obtained.

The growth results are not sensitive to the variation of ex-situ substrate preparation parameters, RIE and HF etching time. The nanowire growth on native oxide is not as good as on H_2O_2 created oxide layer. The yield of vertical nanowires shows hole diameter dependence, the highest yield, around 90%, being obtained for arrays with the hole diameter 20nm and 40nm. The trends of nanowire length and diameter with increasing growth time are also investigated extracting a growth rate of 940nm/h. The change from competitive growth regime to diffusion limited regime happens at pitch 2μm, which is the same as in [28]. In the future, it will be useful to investigate how to make the InAs nanowire length distribution narrower. An idea is to obtain the right and uniform size of pinholes through optimizing the temperature in the surface modification procedure.

In addition, the in-situ passivation of InAs nanowire arrays by ALD of Al_2O_3 was successfully demonstrated.

InAs/$Al_{0.6}Ga_{0.4}Sb$ core shell nanowires were grown by MBE with different shell growth time and investigated by EDX and TEM. From TEM measurements, the shell growth rate was estimated. In the future, InAs/$Al_{0.6}Ga_{0.4}Sb$ core-shell nanowires can be grown using Ga droplet assisted substrate modification procedure and more detailed TEM characterization is necessary for the shell thickness information.

Finally, InAs nanowire-array based devices were fabricated, in which HSQ serves as the support and planarization layer. The DC electrical characteristics at room temperature of unpassivated InAs nanowire and Al_2O_3 passivated InAs nanowire arrays were investigated. The I-V characteristics are linear in both cases demonstrating that the deices have good Ohmic contacts. After the resistivity calculation, it can be concluded that in average, the resistivity of Al_2O_3 passivated InAs nanowires is lower than the one of unpassivated InAs nanowires.

A problem in the device fabrication process is that the HSQ quality was not good enough after RTP treatment at 300°C/15min. The HSQ annealing at 400°C for 1hour was also not very successfully. In the future, it can be further investigated how HSQ behaves after annealing at 300°C for longer time, e. g. for 1 hour. Another idea is to use electron beam lithography instead of high temperature treatment, as electron beam can also lead to cross-linkage of HSQ.

Bibliography

[1] S. Mokkapati and C. Jagadish, “III-V compound SC for optoelectronic devices,” *Mater. Today*, vol. 12, no. 4, pp. 22–32, 2009.

[2] “Ioffe Institute. New Semiconductor Materials, Characteristics and Properties.” [Online]. Available: http://matprop.ru/.

[3] S. A. Shaikh, “Emerging III-V Semiconductor Compound Materials for Future High-Speed and Low Power Applications : A Review and Challenges,” *Int. J. Innov. Res. Sci. Technol.*, vol. 6, no. 2, pp. 1929–1935, 2017.

[4] L. Wernersson, M. Hong, A. Jesus, H. Riel, L. Wernersson, and M. Hong, “III – V compound semiconductor transistors — from planar to nanowire structures,” *MRS Bull.*, vol. 39, no. 02, pp. 668–677, 2014.

[5] K. J. Kuhn, “Considerations for Ultimate CMOS Scaling,” *IEEE Trans. Electron Devices*, vol. 59, no. 7, pp. 1813–1828, 2012.

[6] G. Koblmüller *et al.*, “Self-induced growth of vertical free-standing InAs nanowires on Si(111) by molecular beam epitaxy,” *Nanotechnology*, vol. 21, no. 36, 2010.

[7] H. Schmid *et al.*, “III-V semiconductor nanowires for future devices,” *Des. Autom. Test Eur. Conf. Exhib.*, pp. 1–2, 2014.

[8] K. E. Moselund, H. Schmid, C. Bessire, M. T. Bjork, H. Ghoneim, and H. Riel, “InAs-Si nanowire heterojunction tunnel FETs,” *IEEE Electron Device Lett.*, vol. 33, no. 10, pp. 1453–1455, 2012.

[9] A. G. Milnes and A. Y. Polyakov, “Indium arsenide: a semiconductor for high speed and electro-optical devices,” *Mater. Sci. Eng. B*, vol. 18, no. 3, pp. 237–259, Apr. 1993.

[10] S. A. Dayeh, D. P. R. Aplin, X. Zhou, P. K. L. Yu, E. T. Yu, and D. Wang, “High electron mobility InAs nanowire field-effect transistors,” *Small*, vol. 3, no. 2, pp. 326–332, 2007.

[11] A. Sadao, *Physical Properties of III-V Semiconductor Compounds - InP, InAs, GaAs, GaP, InGaAs, and InGaAsP*. John Wiley & Sons, 1992.

[12] M. Koguchi, H. Kakibayashi, M. Yazawa, K. Hiruma, and T. Katsuyama, “Crystal Structure Change of GaAs and InAs Whiskers from Zinc-Blende to Wurtzite Type,” *Jpn. J. Appl. Phys.*, vol. 31, no. 7 R, pp. 2061–2065, 1992.

[13] K. A. Dick, C. Thelander, L. Samuelson, and P. Caroff, “Crystal Phase Engineering in Single InAs Nanowires,” 2010.

[14] L. Olsson, C. B. M. Andersson, M. C. Håkansson, J. Kanski, L. Ilver, and U. O. Karlsson, “Charge accumulation at InAs surfaces,” *Phys. Rev. Lett.*, vol. 76, no. 19, pp. 3626–3629, 1996.

[15] C. Blömers, “Electronic Transport in Narrow-Gap Semiconductor Nanowires,” PhD thesis, Jülich Research Centre PGI-9, 2012.

[16] P. Woodall, J. M., Freeouf, J.L., Pettit, G.D., Jackson, T., Kirchner, “Ohmic contacts to nGaAs using graded band gap layers of Ga1-xInxAs grown by MBE,” *J. Vac. Sci. Technol.*, vol. 19, pp. 626–627, 1981.

[17] Ö. Gül, “Phase-coherent transport in GaAs/InAs core-shell nanowires,” PhD thesis, Jülich Research Centre PGI-9, 2012.

[18] S. A. Dayeh, C. Soci, P. K. L. Yu, E. T. Yu, and D. Wang, “Transport properties of InAs nanowire field effect transistors: The effects of surface states,” *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.*, vol. 25, no. 4, p. 1432, 2007.

[19] J. W. W. Van Tilburg, R. E. Algra, W. G. G. Immink, M. Verheijen, E. P. A. M. Bakkers, and L. P. Kouwenhoven, “Surface passivated InAs/InP core/shell nanowires,” *Semicond. Sci. Technol.*, vol. 25, no. 2, 2010.

[20] W. R. F. Norman G. Einspruch, *Heterostructure and Quantum Well Physics*, vol. 24. Elsevier, 1994.

[21] J. W. Matthews and A. E. Blakeslee, “Defects in epitaxial multilayers: I. Misfit dislocations,” *J. Cryst. Growth*, vol. 27, pp. 118–125, 1974.

[22] T. Rieger, D. Grützmacher, and M. I. Lepsa, “InAs nanowires with AlxGa1-xSb shells for band alignment engineering,” *J. Cryst. Growth*, vol. 425, pp. 80–84, 2015.

[23] T. Rieger, “Growth and structural characterization of III-V semiconductor nanowires,” PhD thesis, Jülich Research Centre PGI-9, 2015.

[24] N. A. Güsken, “MBE growth and characterization of Te-doped InAs nanowires and InAs / superconductor hybrid structures,” Master thesis, Jülich Research Centre PGI-9, 2016.

[25] H. C. M. Knoops, S. E. Potts, A. A. Bol, and E. Kessels, *Atomic Layer Deposition*. Elsevier, 2015.

[26] “3.1.6.2 Schottky Contact.” [Online]. Available: https://www.iue.tuwien.ac.at/phd/ayalew/node56.html.

[27] G. P. Nagda, “MBE growth and characterization of InAs / GaSb core / shell nanowire arrays,” Master thesis, Jülich Research Centre PGI-9, 2019.

[28] D. K. A. Gurunathan, “III-V core-shell nanowires for low power electronic devices,” Master thesis, Jülich Research Centre PGI-9, 2017.

[29] T. Grap, T. Rieger, C. Blömers, T. Schäpers, D. Grützmacher, and M. I. Lepsa, “Self-catalyzed VLS grown InAs nanowires with twinning superlattices,” *Nanotechnology*, vol. 24, no. 33, pp. 1–7, 2013.

[30] T. Rieger, D. Grützmacher, and M. I. Lepsa, “Si substrate preparation for the VS and VLS growth of InAs nanowires,” *Phys. Status Solidi - Rapid Res. Lett.*, vol. 7, no. 10, pp. 840–844, 2013.

[31] S. Hertenberger, “Growth and Properties of In(Ga)As Nanowires on Silicon,” PhD thesis, Technical University of Munich, 2012.

[32] S. Hertenberger *et al.*, “Rate-limiting mechanisms in high-temperature growth of catalyst-free InAs nanowires with large thermal stability,” *Nanotechnology*, vol. 23, pp. 1–12, 2012.

[33] J. Knoch and J. Appenzeller, “Modeling of High-Performance p-Type III-V,” vol. 31, no. 4, pp. 305–307, 2010.

[34] T. Tauchnitz *et al.*, “Decoupling the two roles of Ga droplets in the self-catalyzed growth of GaAs nanowires on SiOx/Si(111) substrates,” *Cryst. Growth Des.*, vol. 17, no. 10, pp. 5276–5282, 2017.

[35] T. Tauchnitz, Y. Berdnikov, V. G. Dubrovskii, H. Schneider, M. Helm, and E. Dimakis, “A simple route to synchronized nucleation of self-catalyzed GaAs nanowires on silicon for sub-Poissonian length distributions,” *Nanotechnology*, vol. 29, no. 50, p. 504004, 2018.

[36] H. K. Paul and Jacob， Broder, “The Solubility of Silicon and Gerraanium in Gallium and Indium,” *Phys. Rev.*, vol. 90, no. 4, p. 521, 1953.

[37] U. Neuwald, A. Feltz, U. Memmert, and R. J. Behm, “Chemical oxidation of hydrogen passivated Si(111) surfaces in H2O2,” vol. 78, no. 6, pp. 4131–4136, 1995.

[38] C. Heyn, “Kinetic model of local droplet etching,” *Phys. Rev. B - Condens. Matter Mater. Phys.*, vol. 83, no. 16, pp. 1–5, 2011.

[39] T. Miura, M. Niwano, D. Shoji, and N. Miyamoto, “Kinetics of oxidation on hydrogen-terminated Si (100) and (111) surfaces stored in air,” vol. 4373, 1996.

[40] “Manipulator.” [Online]. Available: http://www-old.mpi-halle.mpg.de/department2/fileadmin/user_upload/Research_Projects/Nanowires___Nano objects/Si___Ge_Nanowhiskers_by_MBE/Equipment/manipulator.html.

[41] M. Zhao, B. Chen, C. Xie, M. Liu, and J. Nie, “Study of process of HSQ in electron beam lithography,” in *2010 IEEE 5th International Conference on Nano/Micro Engineered and Molecular Systems*, 2010, pp. 1021–1024.

[42] M. J. Loboda and G. A. Toskey, “Understanding hydrogen silsesquioxane-based dielectric film processing,” *Solid State Technol.*, vol. 41, no. 5, pp. 99–105, 1998.

[43] H. C. Liou and J. Pretzer, “Effect of curing temperature on the mechanical properties of hydrogen silsesquioxane thin films,” *Thin Solid Films*, vol. 335, no. 1–2. pp. 186–191, 1998.

[44] C. C. Yang and W. C. Chen, “The structures and properties of hydrogen silsesquioxane (hsq) films produced by thermal curing,” *J. Mater. Chem.*, vol. 12, no. 4, pp. 1138–1141, 2002.

[45] S. P. Jeng, K. Taylor, T. Seha, M. C. Chang, J. Fattaruso, and R. H. Havemann, “Highly porous interlayer dielectric for interconnect capacitance reduction,” *Dig. Tech. Pap. - Symp. VLSI Technol.*, vol. 337, no. 1994, pp. 61–62, 1995.

[46] “ImageJ.” [Online]. Available: https://imagej.net/Welcome.

Acknowledgments

First, I would like to thank Prof. Detlev Grützmacher for giving me the opportunity to accomplish my master thesis in our institute in Jülich Research Centre. I would like to express my gratitude to Dr. Mihail Ion Lepsa for providing me this project to investigate III-V semiconductor nanowires, for the guidance during my whole master thesis period, as well as for many useful discussions. Specially, I am grateful to Prof. Regina Dittmann for accepting to be my supervisor at RWTH University.

I would like to thank Christoph Krause and Benjamin Bennemann for keeping the MBE system running smoothly, and for introducing the MBE operational method to me and helping me when I meet problems in Nanocluster.
I would like to thank Soraya Karimzadah for helping me with MBE operation, ALD passivation, and also kind encouragement.
I would like to thank Pujitha Perla for introducing me the spin-coating, RIE process at the beginning.
I would like to thank Jin Hee Bea for the TEM measurements.
I also would like to thank the HNF staff for their support during my substrate preparation and device fabrication process. I would like to thank Dr.Elmar Neumann (for EDX measurments and SEM), Stefan Trellenkamp and Florian Lentz (for electron beam lithrography), Marvin Dollendorf (for dicing), Anja Zass (for AFM measurements), Sven Clausen (for Maskless Aligner 100), Rainer Benzcek and Janine Worbs (for metallization), and Jhih-Sian Tu (for probe station and kind suggestions when I met any experimental problems).

At the end, I would like to thank my family and my friends for supporting me in this special year.